

## ORDER OF MANUFACTURING

- |                    |            |
|--------------------|------------|
| 1. POWER WIRING    | A-550-0-4  |
| 2. GROUNDS         | A-550-0-9  |
| 3. COMPONENTS LIST | A-550-0-11 |
| 4. LOGIC WIRING    | A-550-0-2  |
| 5. TERMINATOR LIST | A-550-0-6  |
| 6. CABLE LIST      | A-550-0-3  |

DRAWN <b>P.J. Priest</b> 1-30-64		<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		TITLE <b>INDEX WIRING LIST</b>	
CHECKED <b>J. O'Leary</b> 3/27/64					
ENG <b>L.C. Stockford</b>		APP'D	REV.	FOR DECO TAPE CONTROL 550 0V4 1964	
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD NOT BE REPRODUCED.		DWG NO. <b>A-550-0-1</b>	ECO. NO. REV. LTR.	REV. LTR.	
				<b>A</b>	
		SHEET	OF	CODE <b>WL</b>	

**digital**

EQUIPMENT  
CORPORATION

MAYNARD, MASSACHUSETTS

# MASTER DRAWING LIST

CODE	DWG. NO.	REV.	NO. OF SHEETS	TITLE
PRODUCTION DWG'S (MECH)				
FPL	C-550-0-1	B	1	DEC - TAPE CONTROL 550
PL	A-550-0-1	B	2	DEC - TAPE CONTROL 550 PARTS LIST
MA	E-10800	B	1	1914 MTG PANEL
PL	A-10800	B	2	1914 MTG PANEL PARTS LIST
MD	C-01493	D	1	5 1/4 PLUG PANEL REWORKED
MD	C-01492	C	1	COVER PLATE
PRODUCTION DWG'S ELEC				
MPL	A-550-0-5	E	1	MODULE PROCUREMENT LIST
ML	A-550-0-10	E	1	MODULE LOCATION-MODULE JUMPERING
S	A-550-0-7	C	1	SPECIAL WIRING INSTRUCTION
MA	A-550-0-8	D	1	PANEL LAYOUT ASS'Y.
CD	D-550-0-CD	B	1	DEC - TAPE 550 CONTROL INTERCONNECTING
CD	SD 550-0-16		1	HEAD A CABLE
CD	SD 550-0-17		1	SECTION C CABLE
CD	SD 550-0-18		1	SECTION F CABLE
CD	SD 550-0-19		1	HEAD B CABLE
PW	D-550-0-PW	B	1	POWER WIRING & INDICATOR LITE WIRING
CD	D-550-0-CD		1	INTERCONNECTING CABLES
PL	A-550-0-CD	A	1	DEC TAPE 550 CONTROL INTERCONNECTING CABLES
BD	D-550-0-BD	C	1	CHECKOUT & SERVICE DWG'S
BS	D-550-0-C1	F	1	BLOCK DIAGRAM-550 CONTROL
BS	D-550-0-C2	F	1	C1 CONTROL PRINT #1
BS	D-550-0-TM	E	1	C2 FLAG RESPONSE DATA CONTROL OUTPUTS
BS	D-550-0-W	G	1	CONTROL PULSES
BS	E-550-0-1N	E	1	W MARK TRACK & DECODING ERRORS
UML	D-550-0-UML	F	1	IN INFORMATION HANDLING
TD	D-550-0-TD	C	1	UTILIZATION MODULE LIST
TD				TIMING DIAGRAM
REV.	ECO	ENG	DATE	MADE BY 2/3/64 J. Lemoine P.J. Priest
B	185	L.B.P.	2/19/64	CHECKER 2/19/64 D. Healy N. Rheault
C	RETW/PED	D.G.V.	5/1/64	ENG 2/19/64 L. Stockebrand
D	2054	D.G.V	6/18/64	
E	251		6/29/64	
F	2123		8/25/64	
H	281			
G	2133		9/17/64	
TITLE				DEC TAPE CONTROL 550
FOR				• SCHEMATIC IS FURNISHED ONLY FOR TEST • MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.
SHEET 1 OF 2				NOV 4 1964
CODE DWG. NO.				REV. 1
MDL A-550-0-1				1

**digital**EQUIPMENT  
CORPORATION

MAYNARD, MASSACHUSETTS

**MASTER DRAWING LIST**

CODE	DWG NO.	REV.	NO. OF SHEETS	TITLE
CP	A-550-013	A	34	CHECKOUT PROCEDURE <del>DEC TAPE 550 CONTROL</del>
MN	A-550-0-12	A	1	USER DOCUMENTS LIBRARY PUBLICATIONS SPARE PARTS LIST
WL	A-550-0-1	A	1	INDEX WIRING SHEET
CL	A-550-0-3	D	9	IOT CONTROL
PW	A-550-0-4	D	1	POWER WIRING
TL	A-550-0-6	D	3	TERMINATOR LIST
WS	A-550-0-9	D	4	GROUNDS
CD	A-550-0-11	D	3	COMPONENTS LIST
BWC	D-550-0-15	A	1	DEC TAPE 550 INSTALLATION (PDP-4)
CL	A-550-01-00-04-00	B	1	TO INFO. PLUGS 550 CONTROL
CL	A-550-01-00-05-00	B	1	TO CONTROL PLUGS 550 CONTROL
WL	A-550-01-00-05-00	B	1	WIRING IN REAL TIME SECTION
<small>THIS SCHEMATIC IS FURNISHED ONLY FOR TEST &amp; MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE &amp; SHOULD BE TREATED ACCORDINGLY.</small>				
REV.	ECO	ENG	DATE	MADE BY 2/3/64 J. Lemoine P. J. Priest
B	<del>1.0</del>	L. S. P.	2/19/64	CHECKER 2/19/64 D. Healy N. Rheault
C	<del>1.0</del>		6/1/64	ENG 2/19/64 L. Stockebrand
				TITLE DEC TAPE CONTROL 550
				FOR <del>DEC TAPE CONTROL 550</del>
				NOV 4 1964.
				SHEET 3 OF 2 CODE DWG. NO. MDL A-550-0-1 REV. JFT

**digital**EQUIPMENT  
CORPORATION

MAYNARD, MASSACHUSETTS

**MASTER DRAWING LIST**

CODE	DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
<b>PRODUCTION DWG'S (MECH)</b>				
FPL	C-550-0-1	B	1	DEC - TAPE CONTROL 550
PL	A-550-0-1	B	2	DEC - TAPE CONTROL 550 PARTS LIST
MA	E-10800	B	1	1914 MTG PANEL
PL	A-10800	B	2	1914 MTG. PANEL PARTS LIST
MD	C-01493	D	1	5 1/4 PLUG PANEL REWORKED
MD	C-01492	C	1	COVER PLATE
<b>PRODUCTION DWG'S ELEC</b>				
MPL	A-550-0-5	E	1	MODULE PROCUREMENT LIST
ML	A-550-0-10	E	1	MODULE LOCATION-MODULE JUMPERING
S	A-550-0-7	C	1	SPECIAL WIRING INSTRUCTION
MA	A-550-0-8	D	1	PANEL LAYOUT ASS'Y.
WL	B-550-0-16			WIRE LIST TYPE 550 DT
CD	D-550-0-CD	B	1	DEC - TAPE 550 CONTROL INTERCONNECTING
PW	D-550-0-PW	B	1	POWER WIRING & INDICATOR LITE WIRING
PL	A-550-0-CD	A	1	DEC TAPE 550 CONTROL INTERCONNECTING CABLES CHECKOUT & SERVICE DWG'S
BD	D-550-0-BD	C	1	BLOCK DIAGRAM 550 CONTROL
BS	D-550-0-C1	H	1	C1 CONTROL PRINT #1
BS	D-550-0-C2	H	1	C2 FLAG RESPONSE DATA CONTROL OUTPUTS
BS	D-550-0-TM	F	1	CONTROL PULSES
BS	D-550-0-W	H	1	W MARK TRACK & DECODING ERRORS
BS	E-550-0-1N	F	1	IN INFORMATION HANDLING
UML	D-550-0-UML	H	1	UTILIZATION MODULE LIST
TD	D-550-0-TD	C	1	TIMING DIAGRAM
<b>ISSUED</b>				
JAN 18 1965				
REV.	ECO	ENG	DATE	MADE BY 2/3/64 J. Lemoine E. Massarelli
B	185	L.B.P.	2/19/64	CHECKER 2/19/64 D. Healy N. Rheault
C	RETYPEDED	D.G.V.	5/1/64	T. Stockebrand
D	2054	D.G.V.	6/18/64	
E	251	D.G.V.	6/29/64	
F	2123	J.E.S.	8/25/64	
G	281	J.E.S.		
J	2133	E.H.	9/17/64	
K	323	DSV	12/29/64	
SHEET <u>1</u> OF <u>2</u> CODE <u>MDL</u> DWG. NO. <u>A-550-0-1</u>				REV. LET.
				K



**EQUIPMENT  
CORPORATION**  
**MAYNARD, MASSACHUSETTS**

# **MASTER DRAWING LIST**

REV.	ECO	ENG	DATE	MADE BY 2/3/64 J. Lemoine E. Massarelli	CHECKER 2/19/64 D. Healy N. Rheault	ENG 2/19/64 T. Stockebrand	
				TITLE  DEC TAPE CONTROL 550			
				FOR			
				SHEET <u>2</u> OF <u>2</u>	CODE MDL	DWG. NO. A-550-0-1	REV. LET. K

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE COMP	DWG LOCATION	CONT. KEY	S	REMARKS			PAGE	LINE								
D1										TP	50 PIN AMPHENOL		1	1								
DF + EF			D1-2			TWP				GRY/BLK			"	2								
"			ALM ROW 3			"				"			"	3								
++MMRD			D1-4			"				"			"	4								
"			ALF ROW 3			"				"			"	5								
++MMWR			D1-6			"				"			"	6								
"			ALE ROW 3			"				"			"	7								
						"				"			"	8								
						"				"			"	9								
LC + SE			D1-10			"				NOV 4			"	10								
"			ALK ROW 3			"				"			"	11								
MMDF			D1-12			"				"			"	12								
"			ALN ROW 3			"				"			"	13								
MMEF			D1-14			"				"			"	14								
"			ALL ROW 3			"				"			"	15								
POWER CLEAR			D1-16			"				"			"	16								
"			ALR ROW 3			"				"			"	17								
RUN			D1-19			"				"			"	18								
"			ALS ROW 3			"				"			"	19								
- $\frac{1}{4}$ MMSE			D1-21			"				"			"	20								
A1 "			ALG ROW 3			"				REAR OF BLK			"	21								
$\frac{1}{2}$ MMHC			D1-23			"				"			"	22								
"			ALP ROW 3			"				REAR OF BLK			"	23								
MB			D1-25			"				"			"	24								
"			ALF ROW 1			"				"			"	25								

DRAFTSMAN

CHECKED

ENGINEER

WIRING  
SEQUENCECABLE  
LIST

TITLE

10T CONTROL  
DECO TAPE 550 CONTROLECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-3

REV. LTR.

THIS SCHEMATIC IS FOR INFORMATION PURPOSES ONLY. IT IS THE PROPERTY OF THE GOVERNMENT AND IS NOT TO BE COPIED OR REPRODUCED EXCEPT AS AUTHORIZED BY THE CONTRACTING OFFICER.

NOV 4

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN-PIN	ORDER	COLOR VALUE	WIRE COMP	DWG LOCATION	CONT. KEY	S	REMARKS	PAGE	LINE										
DATA FLG ++			D1-26			TWP												GRY/BLK	2	1		
"			ALT ROW 1			"												"	"	2		
BLK FLG ++			D1-27			"												"	"	3		
"			ALS ROW 1			"												"	"	4		
ERROR FLG ++			D1-28			"												"	"	5		
"			ALR ROW 1			"												"	"	6		
OFFEND ++			D1-29			"												"	"	7		
"			ALM ROW 1			"												"	"	8		
MISS ++			D1-30			"												"	"	9		
"			ALN ROW 1			"												"	"	10		
REV ++			D1-31			"												"	"	11		
"			ALK ROW 1			"												"	"	12		
GO ++			D1-32			"												"	"	13		
"			ALJ ROW 1			"												"	"	14		
MKTKER			D1-33			"												"	"	15		
"			ALL ROW 1			"												"	"	16		
UNABLE			D1-34			"											*	"	"	17		
"			ALH ROW 1			"											"	"	"	18		
"			ALI ROW 1			"											"	"	"	19		
"			ALJ ROW 1			"											"	"	"	20		
"			ALK ROW 1			"											"	"	"	21		
"			ALK ROW 2			"											"	"	"	22		
PWR CONTROL			D1-49			"												"	"	23		
"			B-132			"											RED	"	"	24		
GND			D1-50			"											GRY/BLK	"	"	25		

**DRAFTSMAN**  
C. Mazzarelli 1/23/69

## WIRING SEQUENCE

**TITLE**

## LOT CONTROL

DECC TAPE 550 CONTROL

CHECKED  
J. Pleasant 1/23/69

**CABLE  
LIST**

ECO#  
IS D-2133  
WAS C-201

DWG NO.

REV. LTR.

ENGINEER

744

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE COMP							CONT. KEY	S				REMARKS	PAGE	LINE		
D2 JACK FEMALE																	50 PIN AMPHENOL	3	1			
BIT 15	1	-	D2-16			WHT													"	2		
	1	-	C1A ROW 1			"													"	3		
BIT 12	1	-	D2-13			"													"	4		
"	1	-	C1B ROW 1			"													"	5		
BIT 9	1	-	D2-10			"													"	6		
"	1	-	C1C ROW 1			"													"	7		
BIT 6	1	-	D2-7			"													"	8		
"	1	-	C1D ROW 1			"												"	"	9		
BIT 3	1	-	D2-4			"													"	10		
"	1	-	C1E ROW 1			"													"	11		
BIT 0	1	-	D2-1			"													"	12		
"	1	-	C1F ROW 1			"													"	13		
BIT 16	1	-	D2-17			"													"	14		
"	1	-	C1G ROW 1			"													"	15		
BIT 13	1	-	D2-14			"													"	16		
"	1	-	C1H ROW 1			"													"	17		
BIT 10	1	-	D2-11			"	-												"	18		
"	1	-	C1J ROW 1			"													"	19		
BIT 7	1	-	D2-8			"													"	20		
"	1	-	C1K ROW 1			"													"	21		
BIT 4	1	-	D2-5			"													"	22		
"	1	-	C1L ROW 1			"													"	23		
BIT 1	1	-	D2-2			"													"	24		
"	1	-	C1M ROW 1			"													"	25		

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NOV 1 1968

DRAFTSMAN

CHEKED

ENGINEER

WIRING  
SEQUENCE

CABLE  
LIST

TITLE

INFO PLUG TO TAPER PINS  
10T INFORMATION HANDLING

DEC TAPE 550 CONTROL

ECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-3

REV. LTR.

D

	22	23	24	25	36	37	38	39	41	42	44	45	53	5455	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE			WIRE COMP		DWG LOCATION	CONT. KEY	S		REMARKS		PAGE	LINE				
BIT 17	1	-	D2-18		WHT												4	1			
"	1	-	C1N ROW 1		"												"	2			
BIT 14	1	-	D2-15		"												"	3			
"	1	-	C1P ROW 1		"												"	4			
BIT 11	1	-	D2-12		"												"	5			
"	1	-	C1R ROW 1		"												"	6			
BIT 8	1	-	D2-9		"												"	7			
"	1	-	C1S ROW 1		"												"	8			
BIT 5	1	-	D2-6		"												"	9			
"	1	-	C1T ROW 1		"												"	10			
BIT 2	1	-	D2-3		"												"	11			
"	1	-	C1U ROW 1		"												"	12			
MMIOB 15	1	+	D2-34		YEL										PIN HAS 2 WIRES		"	13			
"	1	+	C1A ROW 3		"												"	14			
MMIOB 12	1	+	D2-31		"												"	15			
"	1	+	C1B ROW 3		"										2 WIRES		"	16			
MMIOB 9	1	+	D2-28		"												"	17			
"	1	+	C1C ROW 3		"												"	18			
MMIOB 6	1	+	D2-25		"												"	19			
"	1	+	C1D ROW 3		"												"	20			
MMIOB 3	1	+	D2-22		"										2 WIRES		"	21			
"	1	+	C1E ROW 3		"												"	22			
MMIOB 0	1	+	D2-19		"												"	23			
"	1	+	C1F ROW 3		"												"	24			
MMIOB 16	1	+	D2-35		"										2 WIRES		"	25			
DRAFTSMAN	<i>E. Massarelli 1/23/69</i>				WIRING SEQUENCE				TITLE				INFO PLUG TO TAPER PINS 10T INFORMATION HANDLING DECC TAPE 550 CONTROL								
CHECKED	<i>M. R. Blandy 1/23/69</i>				CABLE LIST								ECO# IS D-2133 WAS C-201	DWG NO.				REV. LTR.			
ENGINEER	<i>ZPK</i>																<i>A-550-0-3</i>				<i>D</i>

THIS SCHEMATIC IS FOR TEST & MAINTAINANCE PURPOSES ONLY. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.

NOV 4 1969

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80	
TITLE	A <sub>c</sub>	P.	RUN PIN	ORDER	COLOR VALUE				WIRE COMP	DWG LOCATION	CONT. KEY	S	REMARKS										
MMI0B-16	1	+	C1G ROW 3		YEL																		
MMI0B-13	1	+	D2-32		"															5	1		
"	1	+	C1H ROW 3		"															"	2		
MMI0B-10	1	+	D2-29		"															"	3		
"	1	+	C1J ROW 3		"														"	4			
MMI0B-7	1	+	D2-26		"														"	5			
"	1	+	C1K ROW 3		"														"	6			
MMI0B-4	1	+	D2-23		"													2 WIRES	"	7			
"	1	+	C1L ROW 3		"														"	8			
MMI0B-1	1	+	D2-20		"														"	9			
"	1	+	C1M ROW 3		"														"	10			
MMI0B-17	1	+	D2-36		"													2 WIRES	"	11			
"	1	+	C1N ROW 3		"														"	12			
MMI0B-14	1	+	D2-33		"														"	13			
"	1	+	C1P ROW 3		"														"	14			
MMI0B-11	1	+	D2-30		"														"	15			
"	1	+	C1R ROW 3		"														"	16			
MMI0B-8	1	+	D2-27		"														"	17			
"	1	+	C1S ROW 3		"														"	18			
MMI0B-5	1	+	D2-24		"													2 WIRES	"	19			
"	1	+	C1T ROW 3		"														"	20			
MMI0B-2	1	+	D2-21		"														"	21			
"	1	+	C1U ROW 3		"													2 WIRES	"	22			
(4) MMB12 <sup>1</sup>	1	+	D2-19		"														"	23			
"	1	+	A1H ROW 3		"														"	24			
DRAFTSMAN	<i>C. Massarelli 1/23/68</i>												WIRING SEQUENCE	TITLE	INFO PLUG TO TAPER PINS 10T INFORMATION HANDLING DEC C TAPE 550 CONTROL								
CHECKED	<i>R. Blawie 1/23/68</i>												CABLE LIST	ECO# IS D-2133 WAS C-201	DWG NO.	A-550-0-3							
ENGINEER	<i>J. E. L.</i>													REV. LTR.									

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST  
& MAINTENANCE PURPOSES. THE CIRCUITS ARE  
PROPRIETARY IN NATURE & SHOULD NOT BE TREATED  
ACCORDINGLY.

NOV 4 1964

	22	23	24	25	36	37	38	39	41	42	44	45	53	5455	56	57	75	76	78	79	80	
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE			WIRE COMP		DWG LOCATION	CONT. KEY	S					REMARKS	PAGE	LINE			
(4) MMB12 <sup>0</sup>	1	+	D2-38		YEL													6	1			
"	1	+	ALJ ROW 3		"													"	2			
GO			D2-31		"													"	3			
"			ALU ROW 3		"													"	4			
REV			D-32		"													"	5			
"			ALT ROW 3		"													"	6			
MODE 1			D2-34		"													"	7			
"			ALV ROW 1		"													"	8			
MODE 2			D2-35		"													"	9			
"			ALU ROW 1		"													"	10			
MODE 3			D2-36		"													"	11			
"			ALV ROW 3		"													"	12			
UNIT SEL 4	1	+	D2-21		"												1014 1964	"	13			
"			ALD ROW 3		"													"	14			
UNIT SEL 3			D2-22		"													"	15			
"			ALC ROW 3		"													"	16			
UNIT SEL 2			D2-23		"													"	17			
"			ALB ROW 3		"													"	18			
UNIT SEL 1	1	+	D2-24		"													"	19			
"			ALA ROW 3															"	20			
GND			D2-50		BLK													"	21			
"			GND		"													"	22			
WRTMR RETURN			B3B		RED													"	23			
"			B4B		"													"	24			
"			A5T ROW 3		"													"	25			
DRAFTSMAN <i>E. Mesarelli</i>	1/23/68				WIRING SEQUENCE	TITLE INFO PLUG TO TAPER PINS IOT INFORMATION HANDLING DEC TAPE 550 CONTROL SELECTION PLUG FROM T.P. BLK.																
CHECKED <i>M. Reault</i>	1/23/68				CABLE LIST	ECO# IS D-2133 WAS C-201	DWG NO.		A-550-0-3		REV. LTR.		<i>D</i>									
ENGINEER <i>Z. Zell</i>																						

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST PURPOSES. THE CIRCUITS ARE SUBJECT TO CHANGE AND ACCORDINGLY ARE NOT PROPRIETARY IN NATURE.

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE COMP	DWG LOCATION	CONT. KEY	S.	REMARKS	PAGE	LIN										
(-15)			B3C		RED													FROM PWR WIRING	7	1		
"			B4C		"														"	2		
"			A5P ROW 3		"														"	3		
GND			B3D		BLK														"	4		
"			B4D		"														"	5		
"			A5R ROW 3		"														"	6		
GO			B3E		WHT														"	7		
"			B4E		"														"	8		
"			A5S ROW 3		"														"	9		
FWD			B3F		"														"	10		
"			B4F		"														"	11		
"			A5M ROW 3		"														"	12		
REV			B3H		"														"	13		
"			B4H		"														"	14		
"			A5N ROW 3		"														"	15		
WR/LOCK			B3J		"														"	16		
"			B4J		"														"	17		
"			A5U ROW 3		"														"	18		
STOP			B3K		"														"	19		
"			B4K		"														"	20		
"			A5A ROW 3		"														"	21		
WRTM LITE			B3L		"														"	22		
" "			B4L		"														"	23		
" "			A5V ROW 3		"														"	24		
UNIT 9			B3N		"														"	25		

DRAFTSMAN  
*E. Massarelli* 1/23/69

CHECKED  
*M. Chauvet* 1/23/69

ENGINEER  
*J. O'Sullivan*

WIRING  
SEQUENCE

CABLE  
LIST

TITLE

SELECTION PLUG FROM T. P. BLK.  
DEC TAPE 550 CONTROL

ECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-3

REV. LTR.

*B*

THIS SCHEMATIC & MAINTENANCE INFORMATION IS FURNISHED ONLY FOR TEST & MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD NOT BE REPRODUCED OR DISCLOSED.

NOV 4 1969

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE			WIRE COMP		DWG LOCATION	CONT. KEY	S		REMARKS		PAGE	LINE					
UNIT 9			B4N		WHT												8	1				
"			A5L ROW 3		"												"	2				
UNIT 8			B3P		"												"	3				
"			B4P		"												"	4				
"			A5K ROW 3		"												"	5				
UNIT 7			B3R		"												"	6				
"			B4R		"												"	7				
"			A5J ROW 3		"												"	8				
UNIT 6			B3S		"												"	9				
"			B4S		"												"	10				
"			A5H ROW 3		"												"	11				
UNIT 5			B3T		"												"	12				
"			B4T		"												"	13				
"			A5G ROW 3		"												"	14				
UNIT 4			B3U		"												"	15				
"			B4U		"												"	16				
"			A5F ROW 3		"												"	17				
UNIT 3			B3V		"												"	18				
"			B4V		"												"	19				
"			A5E ROW 3		"												"	20				
UNIT 2			B3W		"												"	21				
"			B4W		"												"	22				
"			A5D ROW 3		"												"	23				
UNIT 1			B3X		"												"	24				
"			B4X		"												"	25				

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD NOT BE REVEALED.

NOV 4 1964

DRAFTSMAN  
*E. Mazzarelli* 1/23/64

CHECKED  
*H. Beauly* 1/23/64

ENGINEER

WIRING  
SEQUENCE

CABLE  
LIST

TITLE SELECTION PLUG FROM T. P. BLK.  
DECC TAPE 550 CONTROL

ECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-3

REV. LTR.

D

	22	23	24	25	36	37	38	39	41	42	44	45	53	5455	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE COMP	DWG LOCATION			CONT. KEY	S	REMARKS			PAGE	LINE					
UNIT 1			A5C ROW 3		WHT												9	1			
HALT			A5B ROW 3		"													2			
			B3M		"													3			
			B4M		"													4			
																		5			
																		6			
																		7			
																		8			
																		9			
																		10			
																		11			
																		12			
																		13			
																		14			
																		15			
																		16			
																		17			
																		18			
																		19			
																		20			
																		21			
																		22			
																		23			
																		24			
																		25			

DRAFTSMAN

E. Muscarelli 1/23/64

WIRING  
SEQUENCE

TITLE SELECTION PLUG FROM T. P. BLK.  
DEC TAPE 550 CONTROL

CABLE  
LIST

ECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-3

REV. LTR.

ENGINEER

J. Renault 1/23/64

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD NOT BE REPRODUCED ACCORDINGLY.

4074 1964

D

	22	23	24	25	36	37	38	39	41	42	44	45	53	54 55	56	57	75	76	78	79 80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE				WIRE COMP		DWG LOCATION		CONT. KEY	S		REMARKS	PAGE	LINE		
+10V			C21B		BLU								TP			NO CONN TO C20B	1	1		
"			C22B		"												"	2		
"			C23B		"												"	3		
"			C25B		"												"	4		
-15V			C21C		RED											NO CONN TO C20C	"	5		
"			C22C		"												"	6		
"			C23C		"												"	7		
"			C25C		"												"	8		
POWER CONTROL -15V			C11		"												"	9		
"			C118		"											STANOFF	"	10		
"			C18C		"												"	11		
"			C19C		"												"	12		
"			C20C		"												"	13		
"			C24C		"												"	14		
"			C25C		"												"	15		
+10V A2B			A2B		"												"	16		
			A82E		"												"	17		
-15V A3C			A3C		"												"	18		
			A82H		"												"	19		
																	"	20		
																	"	21		
																	"	22		
																	"	23		
																	"	24		
																	"	25		

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD NOT BE TREATED ACCORDINGLY.

NOV 2 1955

DRAFTSMAN  
*E Maggelli 1/23/64*

WIRING  
SEQUENCE

TITLE  
DECO TAPE 550 CONTROL

CHECKED  
*R. Riccioli 1/23/64*

ENGINEER

*J. E. Stoddard 1/23/64*

POWER  
WIRING

ECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-4

REV. LTR.

D

Q-J MODULE NO.

**NO. REQUIRED**

4606	9
4671 "D" MODEL OR LATER	1
4218	1
4102	4
4151 "H" MODEL OR LATER	1
4303	3
4680	2
4105	1
4113	1
1011	5
4127	6
4214	3
4129	1
111	1
4604	1
4115	2
4116	1
4114	1
4117	2
1113	1
4221	1
4261	1
4260	1
4228	6
4301	2
4410	2
4202	1
4401	1
4523	5
1802	1
1105	1
6102	2
1501	1

DRAWN

E. McHugh 12/13/63

CHECKED

ECBED  
M. G. Gault 1/23/62  
G. J. Stoltz 1/24/62

ENG

The logo consists of the word "digital" in a bold, lowercase, sans-serif font, where each letter is enclosed in a separate black rectangular box. Below it, the words "EQUIPMENT CORPORATION" are stacked in a smaller, uppercase, sans-serif font, also within black rectangular boxes.

MOD

TITLE

**MODULE PROCUREMENT LIST**

FOR: DEC TAPE CONTROL 550

DWG NO

REV LTR

1

CODE  
MPL

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.

NOV 4 1964

TITLE	A	P	RUN PIN	ORDER	COLOR	WIRE	DWG LOCATION	CONT. KEY	S	REMARKS	75	76	78
					VALUE	COMP							
8 TERMINATOR			A4S		47 Ω	RES							
"			GND			"							1
9 TERMINATOR			C7Y		47 Ω	"							"
"			GND			"							"
10 TERMINATOR			A19R		22 Ω	"							"
"			GND			"							"
11 TERMINATOR			B9E		47 Ω	"							"
"			GND			"							"
12 TERMINATOR			B11S		22 Ω	"							"
"			GND			"							"
13 TERMINATOR			B11Y		15 Ω	"							"
"			GND			"							"
14 TERMINATOR			B6S		47 Ω	"							"
"			GND			"							"
15 TERMINATOR			B9J		22 Ω	"							"
"			GND			"							"
16 TERMINATOR			B9M		22 Ω	"							"
"			GND			"							"
17 TERMINATOR			A24R		47 Ω	"							"
"			GND			"							"
18 TERMINATOR			B9X		47 Ω	"							"
"			GND			"							"
19 TERMINATOR			B9U		47 Ω	"							"
"			GND			"							"

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NOV 4 1964

DRAFTSMAN

E. Mazzatorta 1/23/64

CHECKED

H. Rheriff 1/23/64

ENGINEER

J. E. Stoddard 1/24/64

201281

WIRING  
SEQUENCE

TERMINATOR  
LIST

TITLE

DEC TAPE 550 CONTROL

ECO#

IS D-2133  
WAS C-201

DWG NO.

A-550-0-6

REV. LTR.

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE			WIRE COMP		DWG LOCATION	CONT. KEY	S					REMARKS	PAGE	LINE			
TERM. A1C1			A2M		47	Ω													2	1		
			GND																	2		
TERM. A1E1			A2S		47	Ω		"											"	3		
			GND					"											"	4		
TERM. A1E1			A3K		39	Ω		"		1NBL									"	5		
			GND					"											"	6		
TERM. A1E1			A3P		47	Ω		"		1NBL									"	7		
			GND					"											"	8		
TERM. A1E1			A3U		47	Ω		"											"	9		
			GND					"											"	10		
TERM. A1E1			A4E		47	Ω		"											"	11		
			GND					"											"	12		
TERM. A1E1			A4M		47	Ω		"											"	13		
			GND					"											"	14		
TERM.			A1S		15	Ω														15		
			GND																	16		
TERM.			A7P		15	Ω														17		
			GND																	18		
TERM.			A3S		39	Ω														19		
			GND																	20		
TERM.			A4K		47	Ω														21		
			GND																	22		
TERM.			B1L1		15	Ω					TMB5									23		
			GND																	24		
			360																	25		

DRAFTSMAN

El. Massarelli 11-23-64

CHECKED

M. Deauill 11-23-64

ENGINEER

WIRING  
SEQUENCETERMINATOR  
LIST

TITLE

DEC TAPE 550 CONTROL

ECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-6

REV. LTR.

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD NOT BE TREATED ACCORDINGLY.

NOV 4

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80	
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE COMP				DWG LOCATION	CONT. KEY	S						PAGE	LINE				
CP SR			C3V		22	Ω				1NB2								3	1				
"			GND																2				
SHIFT SRL			C2U		22	Ω				1NB1									3				
"			GND																4				
SHIFT SR RT			C7Z		22	Ω				1NB7									5				
"			GND																6				
A6R			A6R		10	Ω													7				
			A82R																8				
A6S			A6S		10	Ω													9				
			A82S																10				
A6T			A6T		10	Ω													11				
			A82T																12				
A6U			A6U		10	Ω													13				
			A82U																14				
A6V			A6V		10	Ω													15				
			A82V																16				
A6W			A6W		10	Ω													17				
			A82W																18				
A6X			A6X		10	Ω													19				
			A82X																20				
A6Y			A6Y		10	Ω													21				
			A82Y																22				
A6Z			A6Z		10	Ω													23				
			A82Z																24				
																			25				

DRAFTSMAN

Elaine Massarelli 2/19/64

CHECKED

*E. Massarelli* 2/19/64

ENGINEER

WIRING  
SEQUENCE

TITLE

DEC TAPE 550 CONTROL

TERMINATOR  
LISTECO#  
IS D-2133  
WAS C-201DWG NO.  
A-550-0-6

REV. LTR.

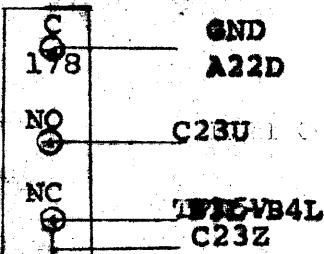
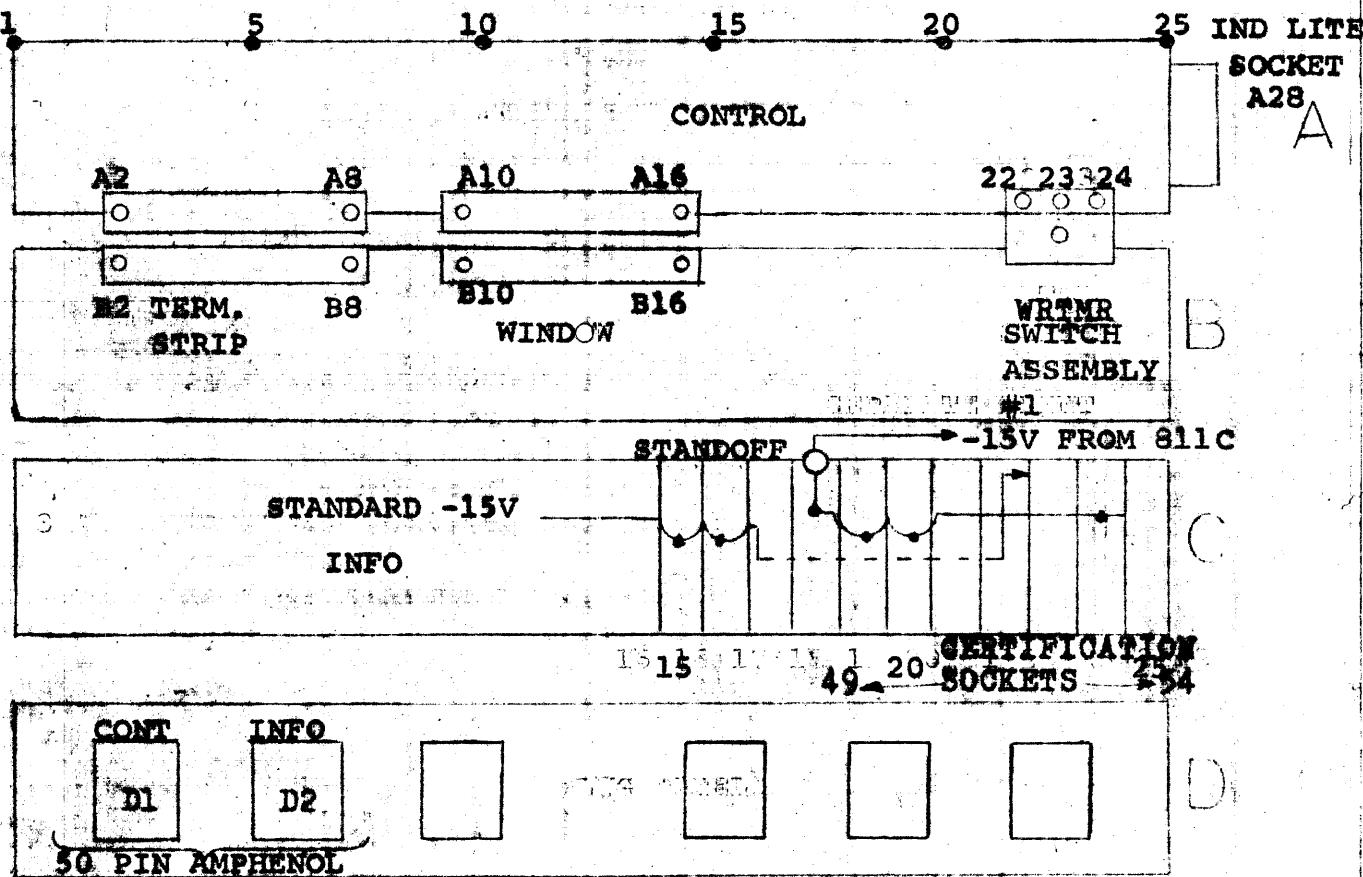
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NOV 4 1964

## SPECIAL WIRING INSTRUCTIONS

1. Run regular -15V to C17C then jump to C23A and stop.
2. There is NO power wiring to pins B3A, B3B, B4A, B4B, and C21A, B, C, C22A, B, C, C23A, B, C. There is -15V wiring to B3C & B4C.
3. Run the +10AV to C20A then jump to C24A and C25A.
4. Run the +10BV to C20B then jump to C24B and C25B.
5. Do not Gnd. B3D or B4D.. These have a special Gnd path.

DRAWN E. McHugh 12/13/63	CHECKED <i>M. Rheault 1/23/64</i>	ENG <i>J. P. Hoad 1/24/64</i>	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				MOD			
				TITLE <b>SPECIAL WIRING INSTRUCTIONS</b>						
				FOR: DEC TAPE CONTROL 550						
				APPRV <i>SPY 114</i>	ECO. NO. <i>4-181</i>	REV. LTR. <i>B-257</i>	DWG NO <i>A-550-0-7</i>	REV. LTR. <i>C</i>		
				SHEET <i>1</i>	OF <i>1</i>		CODE <i>S</i>			
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.				NOV 4 1964	6-2133					



PILOT LIGHT

C23A RED  
-15V

DRAWN

10-23-63

CHECKED

B. Lemphkin 1/23/64  
J. A. Bennett 1/29/64

ENG  
10-23-63  
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.

NOV 4 1964

**digital**  
EQUIPMENT CORPORATION  
MAYNARD, MASSACHUSETTS

APPV  
REV  
D-2133  
809  
1044  
202  
185  
1-185  
251

TITLE

DEC TAPE 550 CONTROL

PANEL LAYOUT

DWG NO

A-550-0-8

REV. LTR.

D

SHEET 1 OF 1

CODE MA

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE COMP							DWG LOCATION	CONT. KEY	S		REMARKS	PAGE	LINE			
A2D			A2D		BLK.											GND.	1		1			
"			A2H		"											"	"	2				
"			A2P		"											"	"	3				
"			A2X		"											"	"	4				
																		5				
A3D			A3D		"											"	"	6				
"			A3J		"											"	"	7				
"			A3R		"											"	"	8				
"			A3W		"											"	"	9				
																		10				
A4D			A4D		"											"	"	11				
"			A4J		"											"	"	12				
"			A4R		"											"	"	13				
"			A4X		"											"	"	14				
																		15				
A11D			A11D		"											"	"	16				
"			A11T		"											"	"	17				
																		18				
A12D			A12D		"											"	"	19				
"			A12T		"											"	"	20				
																		21				
A14D			A14D		"											"	"	22				
"			A14F		"											"	"	23				
"			A14J		"											"	"	24				
"			A14M		"											GND	"	25				

DRAFTSMAN

*E. Wissner 1/23/62*WIRING  
SEQUENCE

TITLE

DEC TAPE 550 CONTROL

CHECKED

*B. Beaumont 1/23/62*

GND

ENGINEER

*J. C. Strodeform 1/23/62*ECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-9.

REV. LTR.

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST  
& MAINTENANCE PURPOSES. THE CIRCUITS ARE  
PROPRIETARY IN NATURE & SHOULD NOT BE REVEALED  
ACCORDINGLY.

NOV 4 1962

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE COMP	DWG LOCATION	CONT. KEY	S	REMARKS	PAGE	LINE										
A14D			A14X		BLK,												GND.	2	1			
"			A14T		"												"	"	2			
A23D			A23D		"												"	"	3			
"			A23R		"												"	"	4			
"			A23X		"												"	"	5			
B6D			B6D		"												"	"	6			
"			B6J		"												"	"	7			
"			B6R		"												"	"	8			
"			B6X		"												"	"	9			
B10D			B10D		"												"	"	10			
"			B10J		"												"	"	11			
"			B10R		"												"	"	12			
"			B10W		"												"	"	13			
B11D			B11D		"												"	"	14			
"			B11J		"												"	"	15			
"			B11R		"												"	"	16			
"			B11W		"												"	"	17			
B12D			B12D		"												"	"	18			
"			B12J		"												"	"	19			
"			B12S		"												"	"	20			
DRAFTSMAN	<i>E Mazzarelli 1/23/69</i>				WIRING SEQUENCE		TITLE		GND'S													
CHECKED	<i>M Rheault 1/23/69</i>				GND		DEC TAPE 550 CONTROL															
ENGINEER	<i>J E A</i>				ECO# IS D-2133 WAS C-201		DWG NO.		A-550-0-9		REV. LTR.											

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD NOT BE REVEALED ACCORDINGLY.

NOV-4 1964

D

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE CDMP	DWG LOCATION			CONT. KEY	S	REMARKS			PAGE	LINE						
B12D			B12V		BLK.											GND.	3	1				
																		2				
B18D			B18D		"												"	"	3			
"			B18H		"												"	"	4			
"			B18T		"												"	"	5			
"			B18X		"												"	"	6			
			B18J		"												"	"	7			
C10D			C10D		"												"	"	8			
"			C10J		"												"	"	9			
"			C10R		"												"	"	10			
"			C10X		"												"	"	11			
																			12			
C11D			C11D		"												"	"	13			
"			C11F		"												"	"	14			
"			C11Z		"												"	"	15			
																			16			
C12D			C12D		"												"	"	17			
"			C12Z		"												"	"	18			
																			19			
C14D			C14D		"												"	"	20			
"			C14F		"												"	"	21			
C15D			C15D		"												"	"	22			
"			C15F		"												"	"	23			
C17D			C17D		"												"	"	24			
"			C17E		"												"	"	25			

DRAFTSMAN

E. Plessenti 1/23/69

WIRING  
SEQUENCE

TITLE

DEC. TAPE 550 CONTROL

GNDS

CHECKED

M. Plessenti 1/23/69

GND

ENGINEER

J. L. A.

ECO#

IS D-2133

WAS C-201

DWG NO.

A-550-0-9

REV. LTR.

D

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.

NOV 4 1969

I	22	23	24	25	36	37	38	39	41	42	44	45	53	54 55	56	57	75	76	78	79 80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE								DWG LOCATION	CONT. KEY	S		REMARKS	PAGE	LINE	
C21E			C21E		BLK											NOT TO C21D	4	1		
"			C21K		"												"	2		
"			C21M		"												"	3		
"			C21S		"												"	4		
"			C21W		"												"	5		
C22E			C22E		"											NOT TO C22D	"	6		
"			C22K		"												"	7		
"			C22M		"												"	8		
"			C22S		"												"	9		
"			C22W		"												"	10		
A16Y			A16Y		"												"	11		
"			GND		"												"	12		
C23J			C23J		"											NO "D" CONNECTION	"	13		
A82F			A82F		"											GND	"	14		
"			GND		"											"	"	15		
"			B62R		"											"	"	16		
B62R			B62S		"											"	"	17		
"			B62T		"											"	"	18		
"			B62U		"											"	"	19		
"			B62V		"											"	"	20		
"			B62W		"											"	"	21		
"			B62X		"											"	"	22		
"			B62Y		"											"	"	23		
"			B62Z		"											"	"	24		
																		25		

DRAFTSMAN

E. Massalotti 1/23/64

CHECKED

M. Beauchet 1/23/64

ENGINEER

20A

WIRING  
SEQUENCE

GND

TITLE

DEC O TAPE 550 CONTROL

GNDs

ECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-9

REV. LTR.

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE &amp; SHOULD NOT BE REPRODUCED.

D

1	
2	4228
3	4228
4	4228 JUMPERS
5	4228 > TO "1"
6	4228 SIDE
7	4228
8	1 1 1 2 2 2 2 2 2
9	4228-13
10	4606 X
11	4301
12	4301
13	4117-R
14	4410
15	4410
16	4302
17	4401
18	4523
19	4523
20	4523
21	HEAD PLUG #1
22	HEAD PLUG #2
23	1802
24	4523
25	4523

4102 - 775  
4680  
SELECT PLUG #1  
SELECT PLUG #2  
4129  
4606 X \*  
1011 2,2,2,2,2,2  
1011 3,4,2,2  
4127-R  
4606 X \*  
4606 X \*  
4604  
4102-R  
4115-R  
4116-L  
4102-R  
4214  
4105  
4117-3  
4115-X  
6102-R  
4221-77/PRESET-  
4127 X \*  
4261  
4260

1501	*
4606 X	*
4606 X	*
4606-R	
4606*	
4671 D	MODEL OR LATER
4218	
4102-R	
4218	
4151 "H"	MODEL OR LATER
4303	
4303	
4680	
1105	
4102-R	
4113-R	
1011 2,2,3,3,2	
4127 X	*
4214	
4127 X	*
1011 2,2,2,2,2,2,	
4127 X	*
4606 R	
4127 X	*
4214	

DRAWN

10423-63

CHECKED

270 VIVES

ENG

ENG

24 Jun 64

The logo for Digital Equipment Corporation (DEC) features the word "digital" in a lowercase, sans-serif font, where each letter is enclosed in a separate black rectangular box. Below it, the words "EQUIPMENT CORPORATION" are stacked in a smaller, all-caps sans-serif font, also within black rectangular boxes. At the bottom, the location "MAYNARD MASSACHUSETTS" is written in a smaller, all-caps sans-serif font.

MOD

JULY E

**MODULE LOCATION-MODUL  
JUMP RING.**

**FOR:** DEC TAPE CONTROL 550

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APPV	ECU	NO.
REV.	LTRF	

Y FOR TEST  
CIRCUITS ARE  
BE TREATED  
~~24~~  
D-2133

DWG NO

REV. LTR.

SHEET 1 OF 1

CODE  
MIL

	22	23	24	25	36	37	38	39	40	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE COMP	DWG LOCATION	CONT. KEY	S	REMARKS			PAGE	LINE								
B15L			B15L			"												1	1			
"			B15C			"												"	2			
B23Y			B23Y			"												"	3			
"			B23C			"												"	4			
DIODE 1			+ A11S															DIODE D-003				
"			- A141															"	9			
DIODE 2			- A11K															DIODE D-003				
"			+ A11D															"	10			
DIODE 3			- B15L															DIODE D-003				
"			+ B115															"	12			
"																		NOV 4 1964	13			
RESISTOR 1			A141															10K OHMS				
"			B11A															"	14			
CAPACITOR 1			A141															CAP 470 MFD				
"			A11K															"	15			
CAPACITOR 2			C9V															CAP .033 MFD				
"			GND															"	16			
CAPACITOR 3			C9Z															"	17			
"			GND															"	18			
DRAFTSMAN	<i>Messarille 1/3/64</i>				WIRING SEQUENCE			TITLE			DEC TAPE 550 CONTROL											
CHECKED	<i>M. Pheault 1/23/64</i>				COMPONENTS LIST			ECO # IS D-2133 WAS C-201			DWG NO.			REV. LTR.			A-550-0-11			D		
ENGINEER	<i>J. Stodderd 2/2/64</i>				SHEET 1 OF 3																	

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*Messarille 1/3/64*

*M. Pheault 1/23/64*

*J. Stodderd 2/2/64*

201-202

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE COMP		DWG LOCATION	CONT. KEY	S	REMARKS		PAGE	LINE								
A2L			A2L		BRN	RES					10K OHMS		2	1								
"			A2C			"															2	
A2T			A2T			"					10K OHMS			3								
"			A2C			"															4	
A4Z			A4Z			"					10K OHMS			5								
"			A4C			"															6	
A18N			A18N			"					10K OHMS			7								
"			A18C			"															8	
B5L			B5L			"					10K OHMS			9								
"			B5C			"															10	
A82E			A82E		BRN	RES					3K 1/2W			11								
			B62E																		12	
A82F			A82F	"		DIODE					003			13								
			B62F																		14	
A82H			A82H	"		RES					1K 1/2W			15								
			B62H																		16	
A82J			A82J	"		DIODE					003			17								
			B62J																		18	
A82K			A82K	"		DIODE					662			19								
			B62K																		20	
A62K			A62K	"		RES					6.8K 1/2W			21								
			A82E																		22	
																					23	
																					24	
																					25	

DRAFTSMAN

*E. Mazzelli 1/23/64*WIRING  
SEQUENCE

TITLE

DEC TAPE 550 CONTROL

CHECKED

*M. Deau 1/23/64*COMPONENTS  
LIST

ENGINEER

ECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-11

REV. LTR.

D

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SHEET 2 OF 3

	22	23	24	25	36	37	38	39	41	42	44	45	53	54	55	56	57	75	76	78	79	80
TITLE	A	P	RUN PIN	ORDER	COLOR VALUE	WIRE COMP	DWG LOCATION	CONT. KEY	S			REMARKS	PAGE	LINE								
CAP. #1			A82R		BRN							.01 MFD. 50V.	3	1								
			B62R									"		2								
CAP. #2			A82S									"		3								
			B62S									"		4								
CAP. #3			A82T									"		5								
			B62T									"		6								
CAP. #4			A82U									"		7								
			B62U									"		8								
CAP. #5			A82V									"		9								
			B62V									"		10								
CAP. #6			A82W									"		11								
			B62W									"		12								
CAP. #7			A82X									"		13								
			B62X									"		14								
CAP. #8			A82Y									"		15								
			B62Y									"		16								
CAP. #9			A82Z									"		17								
			B62Z									"		18								
												"		19								
												"		20								
												"		21								
												"		22								
												"		23								
												"		24								
												"		25								

DRAFTSMAN

WIRING  
SEQUENCE

TITLE

CHECKED

COMPONENT  
LIST

DECOTAPE 550 CONTROL COMPONENTS

ENGINEER

ECO#  
IS D-2133  
WAS C-201

DWG NO.

A-550-0-11

REV. LTR.

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**SPARE PARTS LIST**

QTY	MODEL NO.	TITLE
1	4523	READER WRITER
1	4260	MARK TRACK DECODER
1	4261	MARK SYNC DECODER
1	4671	DECODER

**ONE (1) REPLACEMENT SCHEMATIC AND A DESCRIPTION OF EACH  
OF THE ABOVE MODULES.**

DRAWN  
P.J.Priest 1-31-64

CHECKED

ENG-

**digital**  
EQUIPMENT  
CORPORATION  
MAYNARD, MASSACHUSETTS

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APPV  
A  
REV.  
A-2133

ECO. NO.

REV. LTR.

DWG. NO.  
**A-550-0-12**

SHEET 1 OF 1

REV. LTR.

**A**

CODE  
MN

**SPARE PARTS LIST**

**FOR DEC TAPE CONTROL 550**

# OUTLINE OF DECTAPE CHECKOUT PROCEDURE

## General

### Test Equipment

Tester

Scope

Computer

Test Tapes

Writeups

### ECO Procedure

## Detailed Procedure

### I. Basics

Prints

jumpers

### II. Power

### III. Control Pulses (IOT's)

MMDF

MMEF

MMLL

MMSE

Power Clear

### IV. Selection Control

### V. Motion Control & Mode Selection

Mode Bits & Decoder

GO, REV flops

Start & Reverse Delays

Clear Window

### VI. WRTM MODE

Clock, relay

Error Counter

Preset & Shift pulses

Operation

### VII. WREN FLOP

Operation

Write Interlocking

DRAWN

P.J. Priest 2/28/64

CHECKED

*J. P. Priest* 3/1/64  
ENG *J. P. Priest* 3/1/64

**digital**

EQUIPMENT  
CORPORATION  
MAYNARD, MASSACHUSETTS

TITLE

CHECKOUT PROCEDURE

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APPROV

REV

LTR

DWG NO

A-550-0-13

REV. LTR:

A

SHEET 1 OF 34

CODE  
CP

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A-2133

VIII. Timing Pulses and their derivatives

TPO

TPL

TP2

IX. Information Buffer & Shift Register

Data Flag

MM10B

SR

X. Read Amplifiers/Writers

XI. Mark & Mark Error Detection

Window outputs

Mark Sync outputs

Error Detection

XII. Error Status Conditions

DECTAPE 555/550 CHECKOUT PROCEDURE

Test Equipment:

Scope - Normal CA or other 2 trace presentation scope is enough but a millivolt preamplifier (Type D) and dual shielded direct probe is necessary at Section X. Two scopes - or one dual beam scope - equipped with two millivolt preamps are needed for the skew measurement.

Tester - This consists of -

1. A delay line pulse oscillator which can provide recurrent pulses on the various lines to the tape control. (See sketch with this procedure.)
2. A set of indicators connected to the tape IO buffer.
3. A set of indicators connected to the tape status bit.

DRAWN P.J. Priest 2/28/64	digital						
CHECKED <i>M. Keay 3/9/64</i>	EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				TITLE CHECKOUT PROCEDURE		
ENG <i>J. P. Strode</i>					APPV		
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.					ECO. REV. LTR.	DWG NO A-550-0-13	REV. LTR. A
NOV 4 1964					SHEET 2 OF 34	CODE CP	

4. A pulse generator which is triggered by various "flag up" transitions and which will return a "load buffer" or "unload buffer" (MMWR or MMRD) pulse after a delay.
5. A set of switches to provide mode commands and information via the lines which normally hook to the computer's I/O or AC.
6. The REVERSE and GO command lines can be connected to a complementary flip flop. Many of the foregoing functions can, of course, be provided by a computer. The Microtug programs for the -1 and -4 machines provide the necessary subroutines.
7. A ~~ESCAPE~~ transport is also necessary. It may be provided in the equipment being checked out.

Computer. For actual margins and final bit-by-bit error detection, a computer is necessary. The Microtug subroutines provide the necessary programs. The procedure for checkout with a computer follows this one.

Test Tapes. One tape written with a standard pattern in the mark track and a so-called virgin tape pattern is necessary.

Prints. Before starting checkout procedure it is MANDATORY that one set of block schematics (C1, C2, TM, W, 1, BD, Timing Chart) and the set of production prints that were actually used to manufacture the items be available. (Module location list, wiring list, cable lists, etc.). These must be bound together in some form or another. On these prints all discrepancies will be noted and finally sent along with the machine when checkout is complete.

The basic procedure is to check the operation of the system and in the process generate -

1. A written list of discrepancies

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CHECKED <i>M. Ahnert 3/9/64</i>					TITLE CHECKOUT PROCEDURE		
ENG. <i>J. P. Stoddard</i>		THIS SCHEMATIC IS FURNISHED & MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.	ONLY FOR TEST	APP'V	DWG NO A-550-0-13		REV. LTR. A
		NOV 4 1964	ECO. NO. REV. LTR.	SHEET 3 OF 34		CODE CP	

2. (A marked up) set of block schematics which exactly agree with the equipment.
3. Engineering change orders as appropriate to correct those deficiencies which were present because of incorrect instructions to Production and Checkout. They should also be generated to improve the tester design or overall system reliability.
4. The checkout procedure itself should be updated as design changes and bugs are discovered. It will be used also to revise the Field Test procedure.

One copy of the discrepancies list should be kept permanently by Checkout to assist in checking out further systems. A copy may go along with the prints to the PE or designer. Engineering change orders should be generated as indicated a little further along in this report and will be used to update the present block schematics and plant the seeds for future corrections of the system. These ECO's should be forwarded to the Project Engineer for further processing. Note that these must be forwarded on the same day that the discrepancy was executed if the prints are to be reasonably up to date. At the end of checkout, Quality Control will obtain several brand new sets of prints (which must be on microfilm and listed on the key sheet) and check them against the marked up set to ascertain their accuracy.

ECO Procedure: Checkout originates ECOs for the following reasons in order of urgency.

1. To revise the specific prints applying to the machine
2. To revise the machines which are in process of construction
3. To revise the prints used in construction of future machines (wiring lists, etc.)
4. To revise the prints used in checkout and field maintenance of future machines (block schematics).

DRAWN P.J. Priest 2/28/64		<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
CHECKED <i>M. Pleasant 3/7/64</i>				TITLE	
ENG <i>J.L. Stodder</i>				CHECKOUT PROCEDURE	
THIS SCHEMATIC & MAINTAINANCE IS FURNISHED ONLY FOR TEST PURPOSES. THIS CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.		APP'V	DWG NO	REV. LTR.	
		NOV 4 1964	A-550-0-13	A	
		ECO. NO. LTR.	SHEET 4 OF 34	CODE CP	

5. To update the checkout and test procedures themselves.

The Checkout Department need only originate ECOs (daily). It is up to the Project Engineer or the ECO procedure in Drafting, to follow up and send them wherever they must go. The following items should be mentioned in the ECO form as it is originated. Only the first item is absolutely mandatory - the others are helpful.

EXAMPLE

- |   |  |
|---|--|
| 1. A word description of the change   | Buffers inserted in MMIOB buss                             |
| 2. The wiring that was changed  | Move B 23A from B21A                                       |
| 3. What was actually done to the machine being checked  | Above change done to Serial #69-550                        |
| 4. A reason for the change  | Too much loading on buss                                   |
| 5. The prints affected  | CIB Revision B for Kie and its wiring list                 |
| 6. The machine's effect   | Affects machines after Serial 73, not machines in progress |
| 7. If the change affects machines in progress, rather than future machines, then a detailed description (for the Production girls to execute) of the mod whould be supplied. This is similar to Item 2. |  |

The first item only is mandatory but No. 3 is easy to supply since all prints affected are with the checkout people. No. 7 can, in many cases, be supplied by the checkout people since, in general, they have to modify the current machine already. Machines modified in process will ordinarily not look the same in future production models as in the work in process machines because other mods will go along with those in the future machines and basic wire runs will then be different.

DRAWN P.J. Priest 2/28/64		<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
CHECKED <i>M. McNealit</i> 3/9/64				TITLE	
ENG. <i>JL</i>				CHECKOUT PROCEDURE	
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NOV 4 1964				REV. NO.	DWG NO
					A-550-0-13
					REV. LTR.
					A
				SHEET 5 OF 34	CODE CP

The usual system will be a rack containing a 550 control, some 555 Transports (previously checked out individually before assembly in the rack), a 734 marginal check supply and its control panel and a 728 power supply with a modified 811 power control. In the future, the 555 controls all by themselves should be checked out and sitting on the shelf.

DRAWN P.J. Priest	2/28/64	<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS					
CHECKED <i>M. R. Smith 3/7/64</i>	ENG <i>ZC</i>				TITLE		
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.					CHECKOUT PROCEDURE		
NOV 4 1964	APPV	ECO. NO.	DWG NO	REV. LTR.			
			A-550-0-33	A			
			SHEET 6 OF 34	CODE CP			

## DETAILED CHECK PROCEDURES

(One copy to be filled out and kept with each control)

### 1. BASIC STEPS

#### OBSERVATIONS

A. Check and record on Key Sheet and BLI all serial number, of 550, 555, cabinet assemblies and so on.

CK \_\_\_\_\_

B. Obtain all prints:

1. Prints that were used to produce the items.

2. Checkout prints:

C1, C2, 1, TM, W, BD, 811 Power Control  
Timing Diag. UML.

Consult master print list for correct revisions and see that they exist.

CK \_\_\_\_\_

C. Check that master print list and key sheet adequately cover equipment checked

CK \_\_\_\_\_

D. Check all modules with jumper options against the UML and see that all modules and plugs are installed

CK \_\_\_\_\_

E. Plug in tester and AC power and 555 drive (two wires + AC) if necessary

CK \_\_\_\_\_

DRAWN  
P.J. Priest 2/28/64  
CHECKED  
*M. Neault 3/2/67*  
ENG 79A

**digital**  
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ECO.  
REV.  
LTR.

#### CHECKOUT PROCEDURE

DWG NO

A-550-0-13

REV. LTR.

A

SHEET 7 OF 34

CODE  
CP

F. Remove one end of diode between BISL and A19Z (C2A5) to disable error loop CK \_\_\_\_\_

G. Mark on side of chassis the numbers of all block schematics which apply. CK \_\_\_\_\_

II Power

A. Apply power-watch for smoke

CK \_\_\_\_\_

B. Local remote switch on 811

UP (local) = Power on

DN (Remote) = Power off if -15 switch on tester is off. Check operation (Leave in remote)

CK \_\_\_\_\_

C. Check -15 dump to writers:

**SYNC On -15 switch sync**

jack on tester. When it is turned off -15 at C18C should disappear well before the rest of the -15 from the 728 power supply.

C18C \_\_\_\_\_ MS

D. Measure AC current to 728 and to drives and total current. (Clamp on ammeter)

-15 \_\_\_\_\_ MS

Total \_\_\_\_\_ Amps

728 \_\_\_\_\_ Amps

Drives \_\_\_\_\_ Amps

E. Check marginal check supply output for correctness using a simpson on one back panel and varying the voltage. Compare meter readings.

OK \_\_\_\_\_

DRAWN  
P.J. Priest 2/28/64  
CHECKED

M. Kegel 2/28/64  
ENG 281

**digital**

EQUIPMENT  
CORPORATION

MAYNARD MASSACHUSETTS

TITLE

CHECKOUT PROCEDURE

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APP V

NOV 4 1964

ECO NO.  
REV LTR.

DWG NO

A-550-0-13

REV. LTR.

A

SHEET 8 OF 34

CODE  
CP

### III. CONTROL PULSES

Start tester's delay loop (Fast) to generate continuous pulses on buss to control switches.

Sync on pulse output from delays to buss. The scope \_\_\_\_\_

will remain sync like this all the way to Section IV \_\_\_\_\_  
page 12.

Find pulses on buss for time measurement (expand the time scale to see the pulse well). All buss switches off.

#### A. MMDF and MMEF

1. Select MMDF + MMEF on rotary switch. Check pulse at A3K, S. (C1C4). Change terminator at \_\_\_\_\_ (and record fact) if necessary to reduce Height \_\_\_\_\_ V Term \_\_\_\_\_ O

2. Make MBB12 = 0 with toggle on tester.

Check for -3V at A3T, A4T

Measure MMDF pulse at tester jack. Make MBB12=1; Pulse Gone?

A4T \_\_\_\_\_ V

Height \_\_\_\_\_ V

Quality \_\_\_\_\_

Negat \_\_\_\_\_

3. With MBB12=1 (check +3 at A3L, A4L0

A4L \_\_\_\_\_ V

Check MMEF pulse at tester jack

Height \_\_\_\_\_ V

MBB12=0; Pulse Gone?

Quality \_\_\_\_\_

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CHECKED	W. McNamee 3/1/64	
ENG	20A	

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LTR  
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## III. A.

4. Turn off MMDF + EF for good

Negat \_\_\_\_\_

## B. MMLC + MMSE

1. Turn on "MMLC + MMSE" pulses. Check eight  
 (max. 2.7 same scope syncing on pulse outputs  
of Delay to Buss) and terminate at A4S (C1C3)  
 if necessary.

H \_\_\_\_\_ V  
Q \_\_\_\_\_

Term \_\_\_\_\_

2. With MBB12=0 check MMLC at A18E (C1C5)  
 and change term if > 2.7V (Record fact).  
 Reduce incoming pulse with "substandard"  
 PB on tester and make sure MMLC still exists.  
 Look also for MMLC at A2K (C1B4) Make  
 MBB12=1 and check for no MMLC.

A18E \_\_\_\_\_ V  
Q \_\_\_\_\_  
TERM \_\_\_\_\_  
A2K \_\_\_\_\_  
A2K \_\_\_\_\_

3. Repeat (2). Looking for MMSE at A7P  
 (C1C2) and A2E (C1B3). With MBB12=1  
 check MMSE at A7P (C1C2) and change term  
 if pulse is > 2.7 volts (record fact). Reduce A7P  
 incoming pulse with "substandard" PB on tester A2E  
 and make sure MMSE still exists. Look also for A2E  
 MMSE A2E. (C1B3). Make MBB12=0 and check  
 for no MMSE.

A7P \_\_\_\_\_ V  
Q \_\_\_\_\_  
Term \_\_\_\_\_  
A2E \_\_\_\_\_  
A2E \_\_\_\_\_

Look also for no SE at A2K.

A2K \_\_\_\_\_

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ENG <i>JCN</i>						CHECKOUT PROCEDURE	
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4. Turn off "MMLC + MMSE" pulses. Supply "MMSE" and check its existence at A4E (CLC3). Change A4E \_\_\_\_\_ terminator if necessary to lower pulse to 2.5-2.7V.  
Term \_\_\_\_\_

5. Check output of PA for pulses. (A4H). Turn off A4H \_\_\_\_\_ pulse supply; pulses should stop. A4H \_\_\_\_\_

6. Supply "MMLC" pulses and check A4M (CLC3). Change terminator if necessary. Check output of PA for pulses (A4P) and the look of them. A4M \_\_\_\_\_  
Term \_\_\_\_\_  
A4P \_\_\_\_\_  
A4P \_\_\_\_\_

**Power Clear Pulses**

  - Supply power clear pulses. Check neg amplitude at A3U (CLC4). Change terminator only if really bad. pulse shape A3U \_\_\_\_\_ -V
  - Check pos. amplitude at A19R (CLC5). Change terminator if > 2.7V A19R \_\_\_\_\_ +V  
Term \_\_\_\_\_
  - Check that clear window pulses occur at A4W via B5P and B5M (WD2) A4W \_\_\_\_\_ 1  
B5P \_\_\_\_\_ +V  
B5N \_\_\_\_\_ -V
  - Check that clr status flop pulse exists at A2J (CLB4) Check terminator at \_\_\_\_\_. A2J \_\_\_\_\_ +V  
Term \_\_\_\_\_

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ENG JCA												CHECKOUT PROCEDURE			
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**IV. SELECTION CONTROL**

- A. Supply power clear pulses and MMSE. Set delay times to "Fast".
- B. By changing bits 2, 3, 4, 5 of the "Test Accumulator" switches to one, the flops U4, U3, U2, U1 (in that order) will be set via the in gates and cleared by power clear at A7R. (C1D1)
- C. Check both sides of each flop for rise time (0.2 $\mu$ s rise) and fall time.

R(Y)F R(Z)F

(T) (W)

Continue to sync on buss. (M) (N)

(J) (L)

- D. Insert load plug (ten 100 $\Omega$  resistors to -15) in B3 or B4 or turn selection switch on drive from point to point as check proceeds and check all decoder outputs by going through all the numbers 0-10. Check that each decoder output "waggles" with the correct number in the "AC", by looking at B4 X thru B4N.

D \_\_\_\_\_  
1 \_\_\_\_\_  
2 \_\_\_\_\_  
3 \_\_\_\_\_  
4 \_\_\_\_\_  
5 \_\_\_\_\_  
6 \_\_\_\_\_  
7 \_\_\_\_\_  
8 \_\_\_\_\_  
9 \_\_\_\_\_  
10 \_\_\_\_\_

DRAWN  
P.J. Priest : 2/28/64  
CHECKED  
*M. Mayall 3/3/64*  
ENG *L.A.*

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## V. MODE AND MOTION CONTROL

A. Supply power clear pulses in addition to MMLC.  
Set delays' to "FAST."

### B. Mode

1. By setting test accumulator switch bits 15,16,17 up each "M" flop will be set by MMLC and cleared by power clear at A9R (C1C7). Check all rise and fall times and that correct switch runs correct flop.

Rise/Fall usec  
 (W) M<sub>1</sub><sup>0</sup> - M<sub>1</sub><sup>1</sup> → A9 T  
 (N) M<sub>2</sub><sup>0</sup> - M<sub>2</sub><sup>1</sup> → A9 M  
 (M) M<sub>3</sub><sup>0</sup> - M<sub>3</sub><sup>1</sup> → A9 J

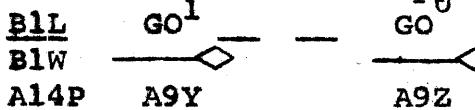
Continue to sync on buss pulse.

- C. 2. Check all 8 decoder for rise and fall by setting all modes in turn. "GO" must be one (bit 12=1) for this test. Temporarily ground A14P to simulate this. Check that outputs disappear when GO=zero.
3. Check the outputs of the inverters at C1B8 which supply the negative levels for assertion when needed.

### C. Motion Flops

#### 1. Go Flop

- (a) by setting Bit 12 the Go flip flop will be set by MMLC and cleared by power clear. Do it. Check Rise and Fall times of Go Flop, and of buffers at



R  
F

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J. Nealey 3/9/64  
ENG S.C.A.

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(b) Check status Bit at tester jack for neg B1L-R B1N-R  
when GO = one via inverter at B13Z (2C2A7) F F  
( right after MMLC pulse). Ignore rise time.

A14P  
R \_\_\_\_\_  
F \_\_\_\_\_

V.C.1. (c) Turn "Run" Switch off on panel and observe that GO flop is held=zero by inverter at A14U (CLC7). Turn "Run" Switch back on.

(d) Turn off power clears and set bit 12 switches on tester to supply a complementing level to Bit 12.

**Continue to sync on buss.** Observe that GO flip flop changes start on each MMLC pulse

B5p

(e) Check that clear window pulses at B5P (WD1) occur at transition of GO to "0".

A4W

## 2. Rev Flop

(a) Turn power clears back on. By setting Bit 13 0 1 switch and Bit 12 the REV flop will be set by MMCL and cleared by power clear. Check rise & fall times of Flop. (CLC6) and of buffers at B13F and B16T. (200 ns max)

Rev → Rev →  
A19V A19T

B13F R \_\_\_\_\_  
F \_\_\_\_\_  
B16T R \_\_\_\_\_  
F \_\_\_\_\_

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ENG	ZD	

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REV.

ECO

NO.

DWG NO

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REV. LTR.

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- (b) Check status bit (at tester) for neg when Rev=1. via inv at B13R (C2A7). Ignore rise time problems
- 
- (c) Turn "Power Clear" off. Turn off bit 12 to clear GO. Observe that rev flip flop goes not change when Bit 13 switch is moved.
- 
- V.C.2. (d) Turn on Bit 12, change Rev to opposite state with Bit 13 and turn 12 back off. Observe that Rev still doesn't budge when Bit 13 switch is moved.
- 

### 3. DELAYS

- (a) Set TESTER TO "SLOW" (2 sec per cycle). Switch Bit 12 transfer switch so that it is supplied from the complementing flip flop. Supply MMLC pulses. GO Flop should alternately set and clear. (Rise time was previously checked).

**SYNC ON BUSS**

- (b) Set START Delay to 150 MS (A12U) (C1A7). A12U  
Check that it fires upon transition of GO to a "one".
- (c) Check output of DIP NOR at A16H. A16H
- (d) Set Tester as in (a) but transfer bit 13 to the complementing line and bit 12 to the test switches. Set test switch 12 go "1" so REV will alternately set and clear at the slow rate.

(e) Test ACQUITY LINE ALSO TESTED AND OK

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ENG <i>ZCA</i>				CHECKOUT PROCEDURE	
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(e) TURN AROUND Delay should be fired at both transitions of REV (at every pulse on the bus). Set it to 250MS., AllU (C1A6)

(f) Check output of DIP NOR AT A16H check rise and fall time because it's used to generate a pulse.

risetime \_\_\_\_\_ / Fall

risetime \_\_\_\_\_ / Fall

(g) Similarly check DIP at B16F (C1A6)

#### D. Drive operation

(a) Load a (SFRATC+1) tape on drive. Generate MMSE select it. Generate MMLC and set TEST SW 12 ( )=1 and 13 to the complementing flop. Drive should run alternately back and forth. Check that direction of motion agrees with status indication. Check for -15 at solenoid drivers Pin E (A13,B2) C1B6 during operation. If drive operation check out SD's and wiring (C1B6).

B2E \_\_\_\_\_

A13E \_\_\_\_\_

(b) Marginal Check -15 and +10 to decoder to drives to check selection and motion relays operation. Should work at least to -11 volts. -15 margins on panel B + 10 on Panel A. What failed?

(c) Remove tape (or let reels spin) for next few sections.

(d) Check enable level due to incorrect selection.

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P.J. Priest 2/28/64  
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*M. Cleland 3/9/64*  
ENG *2C8*

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E. WINDOW Clear

Check clr Window pulses due to both transitions Start \_\_\_\_\_  
of DIP at A4U and Y. See output at A4W. (WD3)

Change sync to DIP output (A16H going to ground)  
to see pulse due to transition at trailing edge.

end \_\_\_\_\_

VI. WRTM MODE

A. Clock Timing Pulses

Set Test Switches to search mode (MMLC and 15-17 = 001).

1. Close Back panel switch to close RELTM relay. Back panel light near switch should light. Red light on drive(s) should light. UP = ON

Relay should close. Check for ground at A16K

A16K

(C2C2) and neg at B7L and B7W.

B7L

See that all three points reverse when switch is turned back off.

B7W

Leave RELTM switch on for remainder of procedure until test tape is mounted for tape operation.

Sync on Clock Pulses.

2. Check Clock output at C17F (TMA1) (positive pulses). \_\_\_\_\_ volts  
Terminate to 2.7 volts or less at A25J if necessary.  
Note term size if new. Set Clock to 8-1/3 psec for new. Turn off RELTM sw and check that clock stops. \_\_\_\_\_ Term size  
\_\_\_\_\_  
Stop?

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CHECKED  
*M. Gaultier 3/1/64*  
ENG  
*JCS*

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CHECKOUT PROCEDURE

R/F

3. (a) Using WRTM waveforms at TMC4 Check Clock  
Flip Flops. CK1' \_\_\_\_\_ /  
CK2' \_\_\_\_\_ /
- (b) Check RECTM at C13T, S (TMC3). (Wiggle  
RELTM switch to make sure). C13T \_\_\_\_\_
- (c) Check TP1 and TP0 at C10P, W (TM34).  
Temporarily ground DIP at C10Z and  
check that TP's disappear. Check at B9X  
and B6S and change terms if >2.7V. C10P \_\_\_\_\_  
C10W \_\_\_\_\_  
C10W \_\_\_\_\_  
C10P \_\_\_\_\_  
  
term \_\_\_\_\_  
de \_\_\_\_\_  
C11E \_\_\_\_\_  
C10H \_\_\_\_\_  
TP2A \_\_\_\_\_  
Term \_\_\_\_\_  
  
Term \_\_\_\_\_  
TP2A \_\_\_\_\_  
term \_\_\_\_\_ ohm  
TP2 \_\_\_\_\_  
term \_\_\_\_\_ ohm
- (d) Check for TP2A at C11E and C10H (TMA5).  
Set delay to 4.5  $\mu$ s. Also look at \_\_\_\_\_  
and \_\_\_\_\_ and change term if necessary  
at \_\_\_\_\_ to reduce pulse to 2.7V.  
Check TP2 at C10H and at C20U change term  
if necessary to reduce pulse to 2.7 volts.

## B. "EK"

1. Set drive number in test SWITCHES 2-5. Generate  
MMSE to select drive. Set UP WRTM MODE (15, 16,  
17 of TEST SWITCHES = 111). Set bit 12 to  
complementing line. Generate MMLC at FAST rate  
to create an "alternating WRTM mode."

Sync again on bus pulses (MMLC)

- (a) Check output of decoder at A10Z (C1B8)  
for proper alternation.

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P.J. Priest 2/28/64  
CHECKED  
J. Priest 3/7/64  
ENG *J.C.S.*

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(b) Check alternating output of WRTMR at A17M - make sure phasing is correct - (C2C2), at A15R (C1B8), and at A17T (C2B3).

A17T

B7M

A17R

B7W

B7K

(c) Change to WRT MODE (011) and check A17K (C2C2) and A17W for proper alternation. Also A17R.

(d) **SYNC ON WRTMR TRANSITIONS** and check preset

pulses at B22Z. (WC2) (Also sync on B23X & Flip RELTM Switch & look for pulses).

(Blk MK should not be present since window has been cleared.)

B22Z

BM

(e) **SYNC ON TPO's at C10W** and check TPO's at B22X.

2. Change from complementing mode to continuous WRTMR mode by selecting TEST bit 12 switch and making it=one.

(a) Find EK6 waveform on print (WB7) EK6  
Check carefully the risetime, and duration. R/F /  
If necessary from now on, jiggle RELTM  
Toggle which should preset the EK if it has been disturbed.

(b) Check same EK6' waveform at A17S and Z. A17S  
(Note notch at Z due to TP2's. (C2C3) A17Z

**SYNC ON leading (NEG) edge WAVEFORM AT  
A17S for rest of procedure.**

DRAWN

P.J. Priest 2/28/64

CHECKED

M. Rheault 3/9/64

ENG

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change term if necessary at \_\_\_\_\_ to  
 reduce pulse to 2.7V  
 Check TP2 at C10H and at C20U  
 change term if necessary to reduce  
 pulse to 2.7 volts.

TP2A \_\_\_\_\_ ohm  
 tem \_\_\_\_\_ ohm  
 TP2 \_\_\_\_\_  
 tem \_\_\_\_\_ ohm

B. "EK"

1. Set drive number in test Switches 2-5.  
 Generate MMSE to select drive. Set up WRTM MODE (15,16,17 of TEST SWITCHES = 111). Set bit 12 to complementing line. Generate MMLC at FAST rate to create an "alternating WRTM mode."

Sync again on bus pulses (MMLC)

- (a) Check output of decoder at A10Z (C1B8) for proper alternation.
- (b) Check alternating output of WRTMR at A17M, make sure passing is correct. (C2C2), at A15R (C1B8), and at A17T (C2B3) (C2B3)

A17T  
 A17M  
 A17R  
 A17W  
 A17K

- (c) Change to WRT MODE (011) and check A17K (C2C2) and A17W for proper alternation. Also A17R.

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(d) **SYNC ON WRTMR TRANSITIONS** and check preset pulses at B22Z. (WC2)  
(Blk MK should not be present since window has been cleared)

B22Z

BM

(e) **SYNC on TPO's at C10W** and check

TPO's at B22X.

2. Change from complementing mode to continuous WRTMR mode by selecting TEST bit 12 switch and making it = one.

(a) Find EK6 waveform on print. (WB7)

EK6

Check carefully the risetime, and duration. If necessary from now on, jiggle RELTM Toggle which should preset the EK if it has been disturbed.

R/F

(b) Check same EK6 waveform at A17S and z.  
(Note notch at Z due to TP2's (C2C3))

A17S

A17Z

**SYNC ON leading (NEG) edge WAVEFORM AT  
A17S for rest of procedure.**

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P.J. Priest 2/28/64  
CHECKED  
*M. Maguire 3/2/64*  
ENG  
*J. C. J.*

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VII. C. WREN FLOP

1. Change back to fast complementing GO mode in WRTM mode so as to alternately clear and set WREN via A17Z and A17W. (C2C3)
  - (a) Set Bit 12 to complementing flop.
  - (b) Set 15,16,17 = 111, Bit 13=0 (FWD)
  - (c) Generate MMLC
  - (d) Disconnect one end error diode at B115 if not already done.
  - (e) Ground (CLIP LEAD) at AZZN to prevent false unable errors from clearing WREN.

2. Check WREN RISE AND FALL TIMES SYNC ON ITSELF

3. SYNC ON BUSS AGAIN

Check that RDF pulses appear at A23W (C2C3)  
(via A24Z) (C2B4) when and only when WRTMR exists. A23W

4. Check that M Break pulses occur at output of A2W (C2A4) for each RDF and that they also occur at tester MB jack.

A2W  
tester

5. Check write interlocking

- (a) Wren level at B13 U,W,S, (C1A5)  
(check rise & fall time carefully)

To see rise times of WREN place on Slow MMLC comp bit up and probe on A19Z the other on B13U when is 1, other is negative.

R F

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CHECKED	J. J. Priest 3/1/64							
ENG	J. J. Priest			APPV	CHECKOUT PROCEDURE			
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- (b) Check neg level at C18,19,20 L via selection and write Lock Switch on drive. (C1A4) Check that ground occurs always on deselecting or WRITE LOCK SWITCH OFF. Repeat for each drive in system. C20L \_\_\_\_\_  
C20L \_\_\_\_\_
- (c) Check neg level at C24, C25 L via RELTM relay C23S, E. (C1A2) \_\_\_\_\_  
\_\_\_\_\_
- (d) Turn off RELTM and check continuity between C24L and ground. \_\_\_\_\_
- (e) Set drive switch to write lock, and observe outputs of C9V and C9Z (C2C7). They should go C9V NEG when WREN and positive otherwise. Remove clip on unable at A22N. No unable failures should occur. C9Z \_\_\_\_\_
- (f) Check Wren Transitions at B16, V,X,Z (C2A2); \_\_\_\_\_  
A21S (TMAS); B8S, P (TMA6); B8F, L (TMC5) \_\_\_\_\_  
\_\_\_\_\_
- (g) B10S, K (TMA7) Neg transitions must be fast \_\_\_\_\_ ns  
ns
- (h) Check SRWB (TEST SW 13 = 0 FOR REV<sup>O</sup> level) Pulse at B10P, B13L, (TMA7) due to wren' transition. 6 TERM \_\_\_\_\_ 0  
( )
- (i) Similarly check for SLWB (TS 13 - 1) at B10H, B13J. (TMA7)  
Check terminators B10H \_\_\_\_\_ 0  
B13J \_\_\_\_\_  
TERM \_\_\_\_\_ ( )
- (j) Slowly comp wren F.F. Rev bit=0. See that B10T is neg. Look for Single pulse at B10P for WREN transition from ground to neg for wren a "1"

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CHECKED <i>H. Priest 3/7/64</i>								
ENG <i>J.C.P.</i>				TITLE				
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.								
NOV 4 1964				APPV	REV.	ECO. NO.	DWG NO	
							A-550-0-13	REV. LTR.
							SHEET 23 OF 34	CODE CP

## VI. D. 3. (b)

- (2) CPW at B11X  
<sub>M</sub>  
 Must disappear if WRTM goes  
 (change to 011 = WRT temporarily) TERM at 0
- (3) TS13 (REV) = 0; MODE (011)  
 FIND SR. at B6P (TMC6)  
 must disappear in WRT (011)  
 mode, with write lock switch in  
 read only, and also with REV = 1.
- (4) TSB (REV) = 1; mode 010 Find  
 SL at B6W (TMC6) - must disappear  
 in WRT with write end switch  
 in read only. And also REV=0.
- (5) Change Search Mode (000)  
 Find MMSR SR at  
 B6P (TMB6) due to  
 B9T (TMB4) and B7Z  
 NEG  
 Check for Disappearance  
 when not search mode
- B11X \_\_\_\_\_  
 B6P \_\_\_\_\_  
 B6P \_\_\_\_\_ WR LOCK  
 B6P \_\_\_\_\_ REV = 1  
 B6W \_\_\_\_\_  
 B6W \_\_\_\_\_  
 B6W \_\_\_\_\_  
 B6P \_\_\_\_\_  
 B9T \_\_\_\_\_  
 B7Z \_\_\_\_\_  
900
- (c) TP2
- (1) Ground LOCK at B24X (WA5) temporarily and see 0-<SR at B11H (TMA5) B11H \_\_\_\_\_  
 TERM \_\_\_\_\_ 0  
 and CPSR at B12H (1 usec pos) (TMA6) B12H \_\_\_\_\_  
 see waveforms on print TERM \_\_\_\_\_ 0

DRAWN P.J. Priest	2/28/64	<b>digital</b> EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS					
CHECKED <i>McPhaul 3/1/64</i>	ENG <i>2C1</i>				TITLE		
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.					APPV	CHECKOUT PROCEDURE	
NOV 4 1964		REV LTR	ECO NO	DWG NO	A-550-0-13		REV. LTR
				SHEET	24	OF 34	CODE CP

- D. 3. (c) (2) In WRTM MODE (111 & GO) RDF pulses at B11S (TMA6) should cause interchange pulses at B11P, (TMA6) every 200  $\mu$ s. if the LOCK jumper is removed B11P from B24X. They should disappear when LOCK short is replaced on B24X. Leave it off when due. Check size of RDF pulses at B11S and terminate if needed to reduce pulse to 2.7 volts B11S \_\_\_\_\_ TERM \_\_\_\_\_ 0
- (3) In WRTM MODE produce FINAL mark by grounding B24T (WA6) B11P should show interchange pulses via B9H and B9F. (TMA5) Remove FINAL ground; interchanges should disappear. Remove B9H \_\_\_\_\_ B9F \_\_\_\_\_
- (4) Ground B24Z (WA6) to produce RBFS pulses by generating prefinal change mode to WRT (011) (TMA6). RBFS should appear at B11M (011) (TMA6) via A23P (C2B1) Terminate if necessary. Check output of interchange at B11P B11M \_\_\_\_\_ TERM \_\_\_\_\_ B11P \_\_\_\_\_

DRAWN P.J. Priest 2/28/64		<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		TITLE	
CHECKED <i>P.O. Howell 3/9/64</i>					
ENG <i>J.C.A.</i>					
<small>THIS CIRCUIT DIAGRAM &amp; MAINTENANCE INFORMATION IS FURNISHED ONLY FOR TEST PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE &amp; SHOULD BE TREATED ACCORDINGLY.</small>					
				APV REV. LTR.	CHECKOUT PROCEDURE
		NOV 4 1964		ECO. NO.	DWG NO A-550-0-13
				SHEET 25 OF 34	REV. LTR. A
					CODE CP

## IX. INFORMATION BUFFER & SHIFT REGISTER

### A., SET UP

Select tape unit and load WRTM status. (Repeat slowly MMLC then MMSE). Put the tape control in RELTM mode via the Toggle switch on the back panel. Tape need not be mounted on drive.

- INAL Then check at C2 - C7Y for MMWR pulse.  
Change terminator only if pulse amplitude is greater than 3 volts.

MMWR \_\_\_\_\_

Term \_\_\_\_\_

### B. SYNC

Synchronize scope on EK<sub>6</sub><sup>1</sup>. This syncing will be maintained throughout the next portion of the procedure. Use the negative leading edge of the square waveform at A17Z to avoid loading the EK<sub>6</sub> flop.

It is convenient to use a dual-trace scope from here on and display the waveform which is present at A17Z (see next paragraph for picture) throughout the next part of the procedure along with the other waveforms which will be viewed.

DRAWN P.J. Priest 2/28/64		<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		TITLE  CHECKOUT PROCEDURE	
CHECKED <i>Not Rebuilt 2/28/64</i>					
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NOV 4 1964				SHEET 26 OF 34	CODE CP

C. DATA FLAG

C2B4 (1) Check existence of MB pulses (Break Request pulses) from pulse generator at ( ). These pulses should cause the delay in tester to operate and return MMWR pulses to C2=C7Y, via tester jack, cable, plug, and taper pin block. MMWR \_\_\_\_\_  
 INAL Change terminator on chocolate block only if greater than 3 volts.

(2) Check MMWR pulse into PA at A2M. Do not change C1 terminator unless pulse is terrible. A2M \_\_\_\_\_  
 Term \_\_\_\_\_

C2B2? (3) Check Clr DF/BF pulses (pos) at A2R. A2R \_\_\_\_\_

(4) Observe Data Flag Flip-Flop at  
 A19X, A19Z A19X /

A19Z /

DRAWN  
 P.J. Priest 2/28/64  
 CHECKED  
*M. Bleau 3/9/64*  
 ENG

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TITLE

CHECKOUT PROCEDURE

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APPRV  
 NO.  
 REV.  
 LTR.

DWG NO

REV. LTR.

A-550-0-13

A

SHEET 27 OF 34

CODE  
 CP

NOV 1 1964

D. MMIOB

(Refer to sketch of IOB waveforms).

With trace of EK6 flop on screen, (if used) use second trace to observe output of each MMIOB bit immediately prior to the interchange pulse.

Ignore other parts of the waveform. With corresponding "Test ACC" switch equal to zero ("0") (down), the MMIOB bit should be ground on the bus. With switch = "1" (up) the bit should be -3 v. prior to interchg.

Note: Bits 2-4, 12-17 will affect mode and selection - turn off MMLC and MMSE pulses when checking these bits.

E. SHIFT REGISTER

With first trace and syncing as before observe the output of each SR bit immediately following the interchange pulse. Ignore other parts of the waveform. With corresponding "ACC" switch = zero (down) the MMSR bit output should be -3 on the appropriate pins of C2-C7. Note: As in bits 2-4, 12-17 will affect mode and selection, so turn off MMSE, MMLC.

MMIOB OUTPUTS TO ACCUMULATORS:

0 / / 9

1 / / 10

2 / / 11

3 / / 12

4 / / 13

5 / / 14

6 / ?? 15

7 / / 16

8 / / 17

DRAWN  
P.J. Priest 2/28/64  
CHECKED  
McNamee 3/9/64  
ENG

**digital**  
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TITLE

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NOV 4 1964

APP'D  
REV. LTR.

DWG NO

A-550-0-13

REV. LTR.

A

SHEET 28 OF 34

CODE  
CP

F. SHIFTING IN TOTAL.

Same syncing as before but with one full cycle of EK6 on screen: Observe SR bit 5, (11), (17) (FWD) 0, (6), (12) (REV).

The switches should affect the waveforms at times indicated in drawing.

DRAWN P.J. Priest 2/28/64		<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				TITLE		
CHECKED <i>M. Chalif 3/9/64</i>						CHECKOUT PROCEDURE		
ENG								
<p>THIS EQUIPMENT IS FURNISHED ONLY FOR TEST PURPOSES. THE CIRCUITS ARE HIGHLY IN FLAME &amp; SHOULD BE TREATED WITH CARE.</p>								
NOV 4 1964				APPRV	ECO. NO.	DWG NO		
					REV. LTR.	A-550-0-13		REV. LTR.
					SHEET 29 OF 34			CODE CP

XI.

C. MARK TRACK AND MARK ERROR FUNCTION

(Rock in Read Mode 2 octal)

WB5 (1) Find "OR" off all marks at B19T and inverse at B20U

Sync on 13E. Notice that exactly two marks are missing (future mode change)

(2) Find EK1 waveform at B20R. Notice off-set.

WC3 At B20R notice offset

(a) Check preset pulses at B22-7

(3) Find @ at B15W notice narrow guard (if CLR window OK)  
Missing RBM - G.

(4) Find window open at B15V

WD1 (a) Check clear window pulses at B5P due to  
guard and mark

(5) Find BMF level at B15U.

(a) Check exact transition times at BM & guard)  
(b) Check

DRAWN  
P.J. Priest 2/28/64

CHECKED

ENG

**digital**  
EQUIPMENT  
CORPORATION  
MAYNARD, MASSACHUSETTS

TITLE

CHECKOUT PROCEDURE

THIS ELECTRONIC EQUIPMENT IS FURNISHED ONLY FOR TEST PURPOSES. THE CIRCUITS ARE  
MAINTENANCE UNUSUAL IN NATURE & SHOULD BE TREATED WITH CARE.

APP'V

ECO. NO.  
REV. LTR.

DWG NO

A-550-0-13

REV. LTR.

A

SHEET 30 OF 34

CODE  
CP

NOV 4 1964

## IX. INFORMATION BUFFER & SHIFT REGISTER

### A. SET UP

Select tape unit and load WRTM status. (Repeat slowly MMSE then MMLC). Put the tape control in RELTM mode via the Toggle switch on the back panel. Tape need not be mounted on drive.

### B. SYNC

Synchronize scope on EK<sub>6</sub><sup>1</sup>. This syncing will be maintained throughout the next portion of the procedure. Use the negative leading edge of the square-waveform at A17Z to avoid loading the EK<sub>6</sub> flop.

It is convenient to use a dual-trace scope from here on and display the waveform which is present at A17Z (see illustration \_\_\_\_\_) throughout the next part of the procedure along with the other waveforms which will be viewed.

NOTE: At this point, experience indicates it would be a good idea to resolder all joints on C2-C7 (Units plugged in).

### C. DATA FLAG

(1) Check existence of MB pulses (Break Request pulses) from pulse generator at (C2A4). These pulses should cause the delay in tester to operate and return MMWR pulses to C2-C7Y, via tester jack, cable, plug, and taper pin block.

MMWR \_\_\_\_\_

Change terminator only if greater than 3 volts.

DRAWN P.J. Priest 2/28/64		<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
CHECKED <i>M. P. Hause 3/19/64</i>				TITLE	
ENG				CHECKOUT PROCEDURE	
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.				APPV	
NOV 4 1964				REV. LTR.	DWG NO A-550-0-13
				ECO. LTR.	SHEET 31 OF 34 CODE CP

- IX. C. (2) Check MMWR pulse into PA at A2M (C1B4). Do not change terminator unless pulse is terrible. A2M \_\_\_\_\_  
 Term \_\_\_\_\_
- (3) Switch briefly to supply MMRD from tester and check A2S and terminate. Check A2R for output. A2S \_\_\_\_\_  
 Term \_\_\_\_\_  
 A2R \_\_\_\_\_ (+V)  
 Term \_\_\_\_\_ R F
- (4) Check Clr DF/BF pulses (pos) at A2R (C1B4). Term if necessary. A19X \_\_\_\_\_  
 A19X \_\_\_\_\_
- (5) Observe Data Flag Flip-flop at A19X, A19Z. It should be set by RDfs via A14L (C2B6) and cleared by clr DF/BF from MMWR.

D. MMIOB

(Refer to sketch of IOB waveforms).

With trace of EK6 flop on screen (if used), use second trace to observe output of each MMIOB bit immediately prior to the interchange pulse. Ignore other parts of the waveform. With corresponding "Test ACC" switch equal to zero ("0") (Down), the MMIOB bit should be ground on the bus. With switch="1" (up) the bit should be -3 V prior to interchg.

MMIOB OUTPUTS TO ACCUMULATOR:

0	/	/	9
1	/	/	10
2	/	/	11
3	/	/	12
4	/	/	13
5	/	/	14
6	/	/	15
7	/	/	16
8	/	/	17

E. SHIFT REGISTER

With first trace and syncing as before observe the output of each SR bit immediately following the interchange pulse. Ignore other parts of the waveform. With corresponding "ACC" switch=zero (down) the MMSR bit output should be -3 on the appropriate pins of C2-C7. Note: As in bits 2-4, 12-17 will affect mode and selection, so turn off MMSE, MMLC.

DRAWN P.J. Priest		2/28/64		<b>digital</b> EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		TITLE	
CHECKED <i>M. J. Priest 3/7/64</i>		ENG					
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NOV 4 1964				APV	ECO.	CHECKOUT PROCEDURE	
				REV.	LTR.	DWG NO A-550-0-13	
				SHEET	32	OF	34
						CODE CP	

F. WRITING WAVEFORMS AT HEADS (WRTM)

G. SHIFTING IN TOTAL

Same syncing as before but with one full cycle of EK6

on screen: Observe SR bit 5, (11) (17) (FWD)

0, (6), (12) (REV).

The switches should affect the waveforms at times indicated in drawing.

X. Set up to read, test read signal, alignment of Amps, rocker, timing pulses WINDOW Read in waveforms.

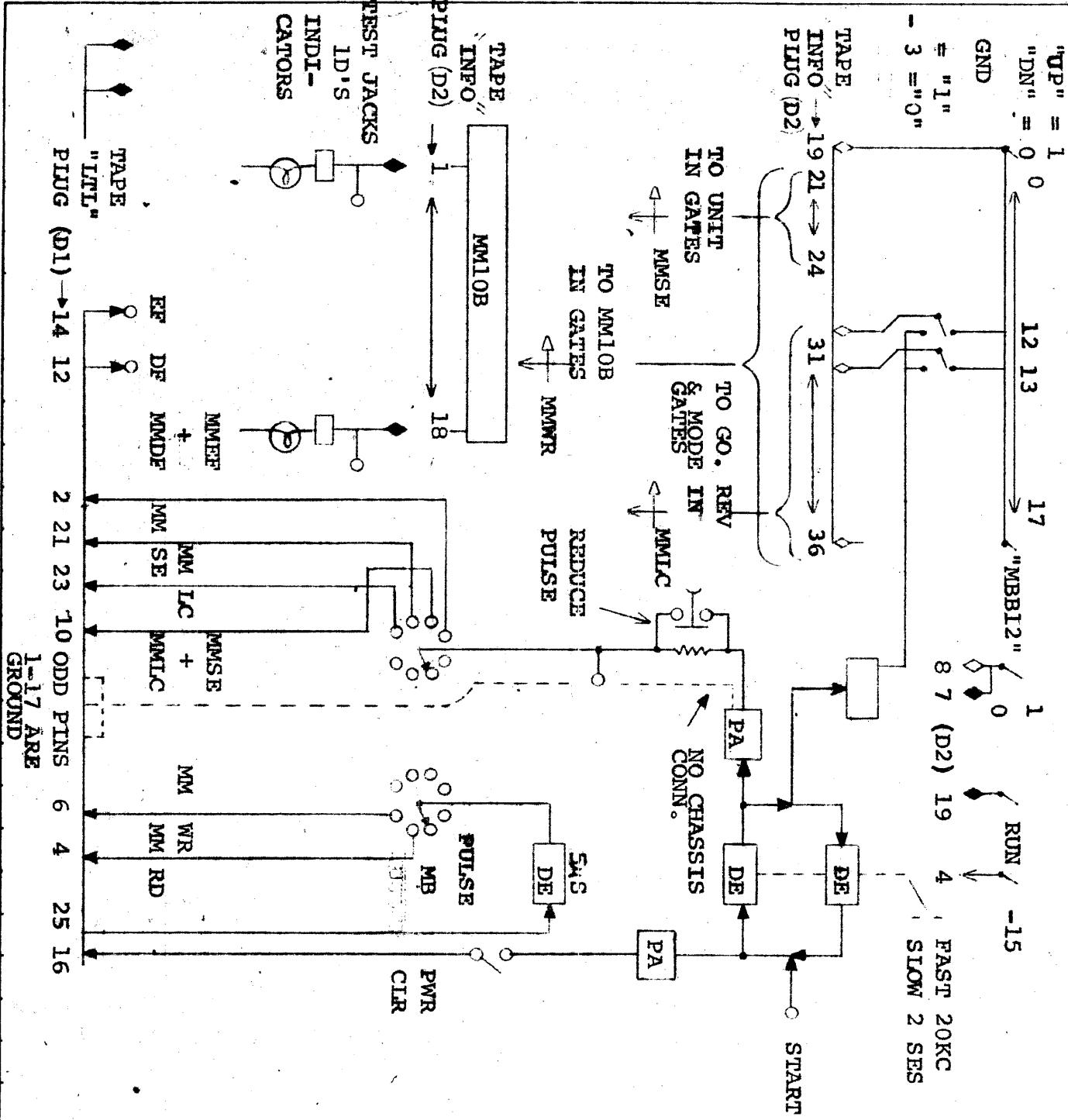
XI.

A. WINDOW OUT

B. ± MARK SYNC OUT

DRAWN P.J. Priest	2/28/64	digital				TITLE			
CHECKED <i>M. Keaull</i>	3/9/64	EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				CHECKOUT PROCEDURE			
ENG						APP'V			
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NOV 4 1964						ECO. NO.	A-550-0-13		
						REV. LTR.	SHEET 33 OF 34		
							CODE CP		

## TEST ACCUMULATOR SWITCHES



DRAWN  
Elaine Massarelli 3/4/64

**CHECKED**  
M. Deauville 3/9/69  
ENG

ENG

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## **CHECKOUT PROCEDURE**

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NOV 4 1984			
	PPV	DWG NO A-550-0-13	REV. LTR. A
	ECO. NO. REV. LTR.	SHEET 34 OF 34	CODE CP

JACK PLUG 

LOCATION, LENGTH, ROUTE

FEMALE MALE 

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
WHITE	2H08X-F1	1	MMIO-0	WHITE	2H03H-F1	26	ACB 7
	2H09X-F1	2	MMIO-1		2H03J-F1	27	ACB 8
	2H10X-F1	3	MMIO-2		2H03K-F1	28	ACB 9
	2H11X-F1	4	MMIO-3		2H03L-F1	29	ACB 10
	2H12X-F1	5	MMIO-4		2H03M-F1	30	ACB 11
	2H13X-F1	6	MMIO-5		2H03N-F1	31	ACB 12
	2H14X-F1	7	MMIO-6		2H03P-F1	32	ACB 13
	2H15X-F1	8	MMIO-7		2H03R-F1	33	ACB 14
	2H16X-F1	9	MMIO-8		2H03S-F1	34	ACB 15
	2H17X-F1	10	MMIO-9		2H03T-F1	35	ACB 16
	2H18X-F1	11	MMIO-10		2H03U-F1	36	ACB 17
	2H19X-F1	12	MMIO-11		2H03V-F1	37	MMB 12
	2H20X-F1	13	MMIO-12	WHITE	2H03W-F1	38	MMB 12
	2H21X-F1	14	MMIO-13			39	
	2H22X-F1	15	MMIO-14			40	
	2H23X-F1	16	MMIO-15			41	
	2H24X-F1	17	MMIO-16			42	
	2H25X-F1	18	MMIO-17			43	
	2H03A-F1	19	ACB 0			44	
	2H03B-F1	20	ACB 1			45	
	2H03C-F1	21	ACB 2			46	
	2H03D-F1	22	ACB 3			47	
	2H03E-F1	23	ACB 4			48	
	2H03F-F1	24	ACB 5			49	
WHITE	2H03G-F1	25	ACB 6	BLK	GND.	50	GND.

DRAWN

Lois Brown 7-3-63

CHECKED

J P Atchison 7-3-63

ENG

J P Atchison

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CORPORATION  
MAYNARD, MASSACHUSETTS

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NOV 4 1964

1-1-20-24-01  
3-5-11-4-49  
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50-11-24-01

50 PIN AMPHENOL

TITLE

TO INFO PLUG OF

550 M.T. CONTROL

REF: 550-01-00-03-00

DWG NO A-550-01-00-04-00 REV. LTR. B

SHEET 1 OF 1 CODE CL

DRAWN  
LOIS BROWN 7-3-63

CHECKED

22

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## **GENERAL WIRING SHEET**

**TITLE**

## 550 TAPE CONTROL:

## WIRING IN REAL TIME SECTION

APP'V ECO. NO.  
REV. LTR.

DWG NO  
A-550-01-00-05-00

REV. LTR.

B

CODE  
W.L.

JACK PLUG 

LOCATION, LENGTH, ROUTE

FEMALE MALE 

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
BLACK	GND	1	GND	WHITE	2H08T-F2	26	DATA F'
GRAY	2F18E-F1	2	IOT 7501		2H09T-F2	27	BLK F'
BLACK	GND	3	GND		2H10T-F2	28	ERR F'
GRAY	2H25S-F1	4	IOT 7502		2H11T-F2	29	OFF END
BLACK	GND	5	GND		2H12T-F2	30	MIS IND
GRAY	2F18K-F1	6	IOT 7504		2H13T-F2	31	REV.
BLACK	GND	7	GND		2H14T-F2	32	GO
GRAY	2H16S-F1	8	IOT 7602		2H15T-F2	33	MK TK ERR
BLACK	GND	9	GND	WHITE	2H16T-F2	34	UNABLE
GRAY	2F19K-F1	10	IOT 7604			35	
BLACK	GND	11	GND			36	
GRAY	2E24W	12	47K TO			37	
BLACK	GND	13	GND			38	
GRAY	2E24U	14	TERMINATORS			39	
BLACK	GND	15	GND			40	
GRAY	2H04B-F3	16	RTO PWR. CLR.			41	
BLACK	GND	17	GND			42	
BLACK	GND	18	GND			43	
GRAY	2H04F-F3	19	RTO BEGIN			44	
BLACK	GND	20	GND			45	
		21				46	
		22		RED	2H05Q	47	+10
		23				48	
		24		BLUE	2H06Q	49	-15
		25		BLACK	GND	50	GND

DRAWN

Lois Brown 7-8-63

CHECKED

J. Blaust 7/9/63

ENG

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**digital**EQUIPMENT  
CORPORATION

MAYNARD, MASSACHUSETTS

50 PIN AMPHENOL

TITLE

TO CONTROL PLUG

(550 M.T. CONTROL)

REF: 550-01-00-02-00

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST &amp; MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE &amp; SHOULD BE TREATED ACCORDINGLY.

B - DWG NO. WAS

APP'V

ECO. NO.  
REV. LTR.DWG NO  
A-550-01-00-05-00REV LTR.  
B

SHEET OF CODE

C.L.

NOV 4 1964

10-24-02  
11/11/63